LSS10020T
IO expander and LED dimming

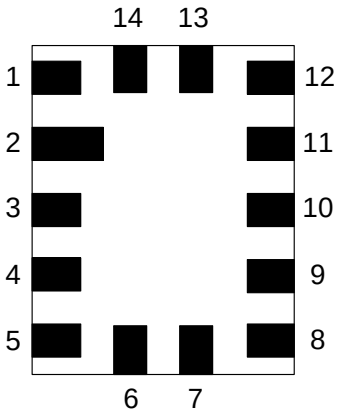
General Description

LSS10020T is a small 14pin QFN packaged customized ASIC with configurable parameters. It support IO expander and LED dimming

Features

- Ultra-low power consumption
- Pb - Free and RoHS Compliant and Halogen - Free
- STQFN - 14 Package

Pin Configuration



1.6mm x 2.0mm 14 Pin STQFN
Top View

Ordering Information

Part Number	Package Type
LSS10020T	14-pin QFN, 3k units Tape and Reel

Program Code Version Information

Date	Datasheet Version	Programming Code Version	Lock Status	Checksum	Part Code	Code Version
2023-12-21	.01	001	L	0XB1EDA639	C26	A

Datasheet Revision History

Date	Version	Change
2023-12-21	0.1	Initial version, new design for LS98102 chip

Reference Schematic

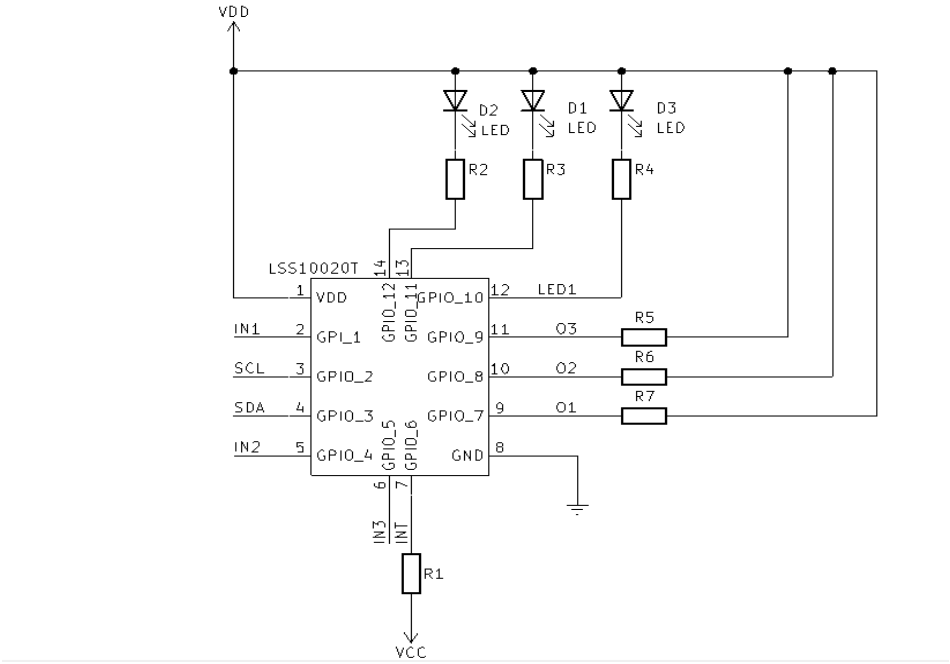


Figure 1. Typical application diagram

Note:

1. Voltage on any pin must be with in GND to VDD.
2. ESD protect is must be considered on all Pins which connected to external interface.

Pin name

Pin	Pin name	TYPE	Function
1	VDD	Power	Power supply input，2.3V~5.5V
2	IN1	Low voltage mode input	Digital signal input 1
3	SCL	Low voltage mode input	I2C SCL
4	SDA	Digital Input/Output	I2C SDA
5	IN2	Low voltage mode input	Digital signal input 2
6	IN3	Low voltage mode input	Digital signal input 3
7	INT	Low voltage mode input	Interrupt output
8	GND	Power	Ground
9	O1	2×open-drain output	I2C Extending IO output 1
10	O2	2×open-drain output	I2C Extending IO output 2
11	O3	2×open-drain output	I2C Extending IO output 3
12	LED1	2×open-drain output	PWM signal output 1
13	LED2	2×open-drain output	PWM signal output 2
14	LED3	2×open-drain output	PWM signal output 3

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
Supply Voltage on VDD to GND	-0.3	7	V
Maximum Voltage Input to Pins	-0.3	7	V
VDD to GND Maximum DC Current	--	90	mA
Input Leakage Current	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (HBM)	2000	--	V
ESD Protection (CDM)	500	--	V
Moisture Sensitivity Level (MSL)	1		

Customize Electrical Characteristics

VDD =3.3V±10%, Temp=25°C

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	Static inputs and floating outputs	--	0.5	--	µA
F_{led}	LED1/2/3	At temperature 25℃		9.7		kHZ
T_{INT}	Delay 1 Time	At temperature 25℃		20		ms

Electrical Characteristics

EC at T = -40°C to +85°C, VDD = 2.3V to 5.5V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.3	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=2.5V	0.8*VDD	--	--	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	0.8*VDD	--	--	V

		Logic Input with Schmitt Trigger, at VDD=5.0V	0.8*VDD	--	--	V
		Logic Input without Schmitt Trigger, at VDD=2.5V	0.7*VDD	--	--	V
		Logic Input without Schmitt Trigger, at VDD=3.3V	0.7*VDD	--	--	V
		Logic Input without Schmitt Trigger, at VDD=5.0V	0.7*VDD	--	--	V
		Low Voltage Input, at VDD=2.5V	0.82	--	--	V
		Low Voltage Input, at VDD=3.3V	0.92	--	--	V
		Low Voltage Input, at VDD=5.0V	1.00	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=2.5V	--	--	0.2*VDD	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	--	--	0.2*VDD	V
		Logic Input with Schmitt Trigger, at VDD=5.0V	--	--	0.2*VDD	V
		Logic Input without Schmitt Trigger, at VDD=2.5V	--	--	0.3*VDD	V
		Logic Input without Schmitt Trigger, at VDD=3.3V	--	--	0.3*VDD	V
		Logic Input without Schmitt Trigger, at VDD=5.0V	--	--	0.3*VDD	V
		Low Voltage Input, at VDD=2.5V	--	--	0.68	V
		Low Voltage Input, at VDD=3.3V	--	--	0.75	V
		Low Voltage Input, at VDD=5.0V	--	--	0.85	V

V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger, at VDD=2.5V	--	0.42	--	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	--	0.45	--	V
		Logic Input with Schmitt Trigger, at VDD=5V	--	0.54	--	V
I_{LKG}	Input leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level OutpuVoltage	Push Pull, 1x Drive I_{OH} = 1mA, at VDD=2.5 V	2.02	--	--	V
		Push Pull, 1x Drive I_{OH} = 3mA, at VDD=3.3 V	2.60	--	--	V
		Push Pull,1x Drive I_{OH} = 5mA, at VDD=5.0 V	4.04	--	--	V
		Push Pull, 2x Drive I_{OH} = 1mA, at VDD=2.5 V	2.10	--	--	V
		Push Pull, 2x Drive I_{OH} = 3mA, at VDD=3.3 V	2.80	--	--	V
		Push Pull, 2x Drive I_{OH} = 5mA, at VDD=5.0 V	4.20	--	--	V
V_{OL}	LOW-Level Output Voltage	Push Pull, 1x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.11	V
		Push Pull, 1x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.25	V
		Push Pull,1x Drive I_{OL} = 5mA, at VDD=5.0 V	--	--	0.29	V
		Push Pull, 2x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.06	V
		Push Pull, 2x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.22	V
		Push Pull, 2x Drive I_{OL} = 5mA, at VDD=5.0 V	--	--	0.21	V
		Open Drain, 1x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.077	V
		Open Drain, 1x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.12	V
		Open Drain, 1x Drive I_{OL} = 3mA, at VDD=5.0 V	--	--	0.15	V
		Open Drain, 2x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.075	V

		Open Drain, 2x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.089	V
		Open Drain, 2x Drive I_{OL} = 3mA, at VDD=5.0 V	--	--	0.114	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push Pull, V_{OH} = VDD-0.2 V, 1X Driver, at VDD=2.5 V	1.37	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 1X Driver, at VDD=3.3 V	5	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 1X Driver, at VDD=5.0 V	19	--	--	mA
		Push Pull, V_{OH} = VDD-0.2 V, 2X Driver, at VDD=2.5 V	2.74	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 2X Driver, at VDD=3.3 V	10	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 2X Driver, at VDD=5.0 V	38	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push Pull, V_{OL} = 0.15 V, 1X Driver, at VDD=2.5 V	1.61	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 1X Driver, at VDD=3.3 V	5	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 1X Driver, at VDD=5.0 V	7	--	--	mA
		Push Pull, V_{OL} = 0.15 V, 2X Driver, at VDD=2.5 V	3.22	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 2X Driver, at VDD=3.3 V	10	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 2X Driver, at VDD=5.0 V	14	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Driver, at VDD=2.5 V	4.9	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Driver, at VDD=3.3 V	15	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Driver, at VDD=5.0 V	21	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Driver, at VDD=2.5 V	9.8	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Driver, at VDD=3.3 V	30	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Driver, at VDD=5.0 V	42	--	--	mA

Oscillators VDD=2.5V						
Power-On time	20MHz OSC	T=+25 °C	--	0.453	--	uS
FreqAccuracy		T=+25 °C	--	19.73	--	MHz
		T=-40 °C to +85 °C	18.352	--	20.336	MHz
Power Consumption		T=+25 °C	--	60	--	uA
		T=-40 °C to +85 °C	--	--	67	uA
Oscillators VDD=3.3V						
Power-On time	20MHz OSC	T=+25 °C	--	0.455	--	uS
FreqAccuracy		T=+25 °C	--	19.90	--	MHz
		T=-40 °C to +85 °C	18.568	--	20.504	MHz
Power Consumption		T=+25 °C	--	73	--	uA
		T=-40 °C to +85 °C	--	--	82	uA
Oscillators VDD=5V						
Power-On time	20MHz OSC	T=+25 °C	--	0.433	--	uS
FreqAccuracy		T=+25 °C	--	20.13	--	MHz
		T=-40 °C to +85 °C	18.784	--	20.776	MHz
Power Consumption		T=+25 °C	--	104	--	uA
		T=-40 °C to +85 °C	--	--	118	uA
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

I2C Communication Interface

LSS10020T provides an I2C communication interface, allowing the I2C master to read or write internal registers, thereby remotely reconfiguring internal resources and their connection relationships.

• I2C Read

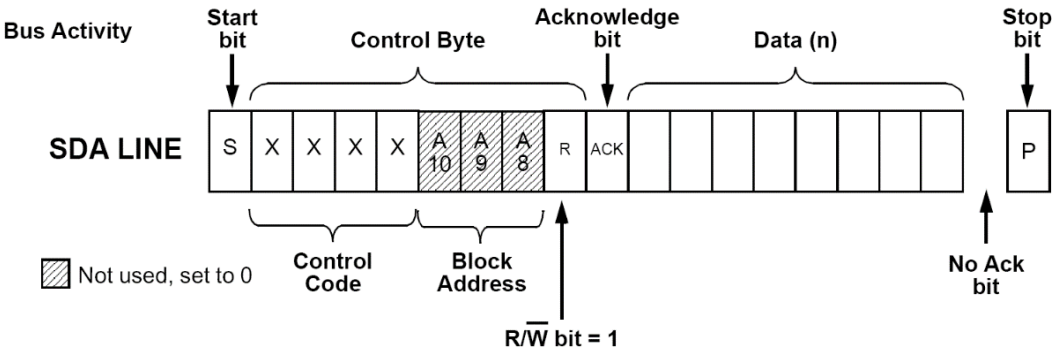


Figure 2. Current Address Read Instruction

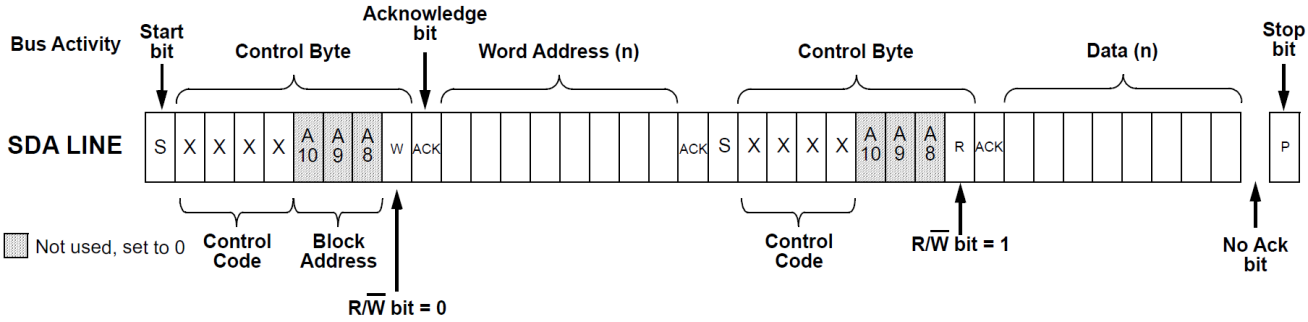


Figure 3. Random Read Instruction

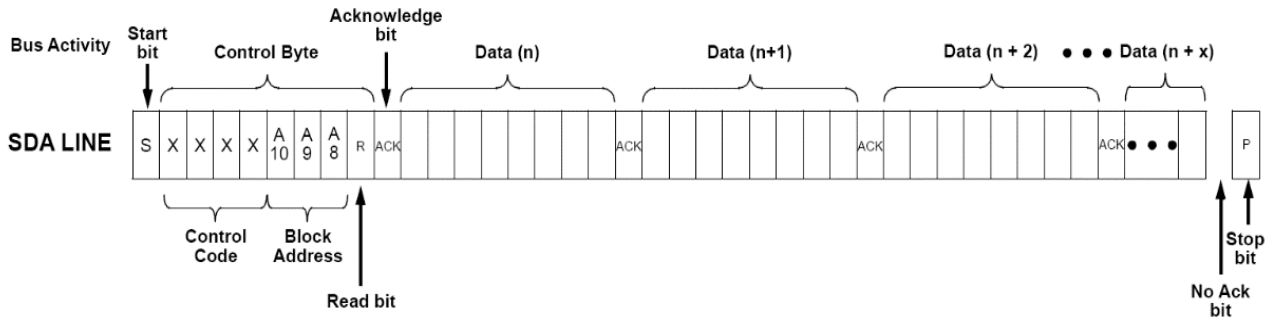


Figure 4. Sequential Read Instruction

• I2C Write

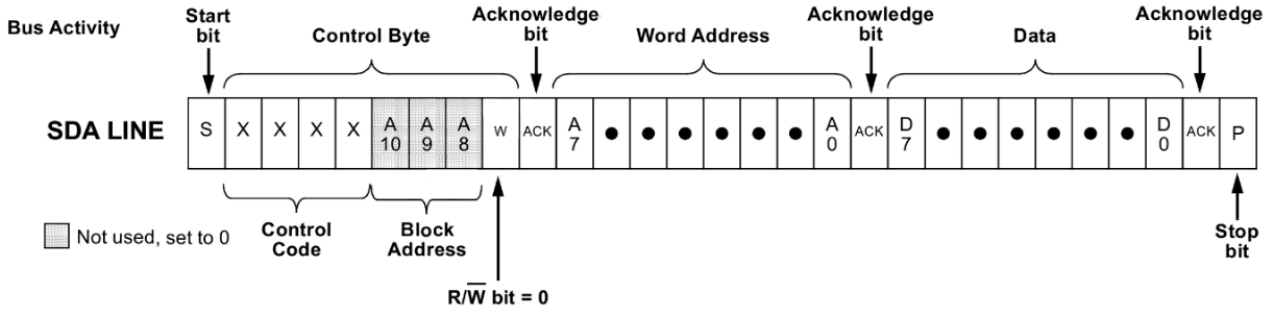


Figure 5. Byte Write Instruction

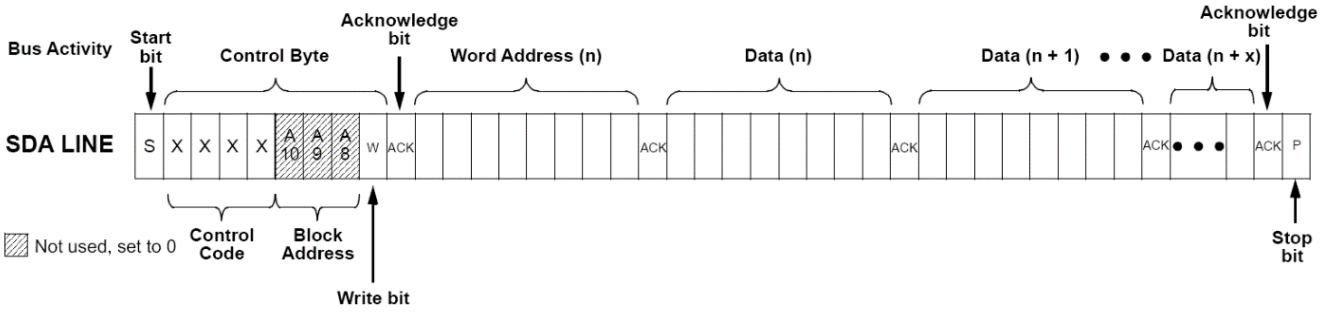


Figure 6. Sequential Write Instruction

• I2C Timing Diagram

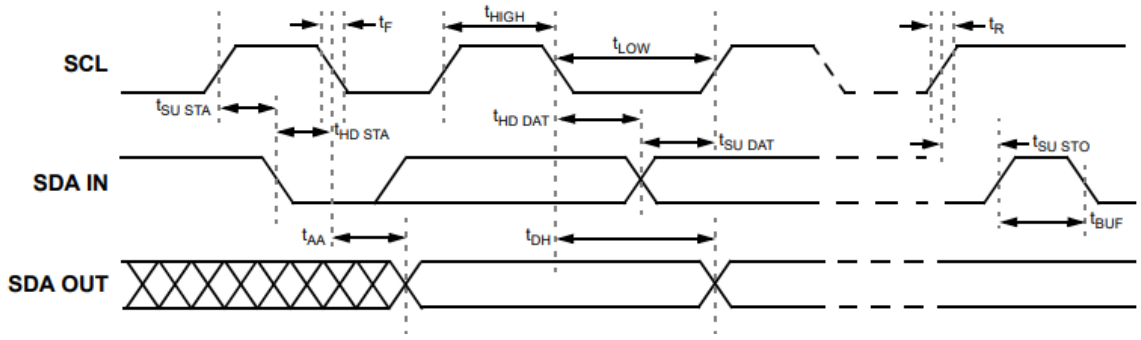


Figure 7. I2C Timing Diagram

I2C operation:

I2C Write command: 0x00, I2C Read command; 0X01

1. Read PIN2/PIN5/PIN6 input status

Step 1: Write Register 0X7E, 00; Write Register 0X7D, 00; Both registers' Default value are 0.

Step2: Read Register 0x7C, the bit vs PIN as below:

Bit：

0	VSS
1	PIN2 Digital Input
2	PIN5 Digital Input
3	PIN6 Digital Input
4	PIN7 Digital Input
5	PIN9 Digital Input
6	PIN10 Digital Input
7	PIN11 Digital Input

2. Set PIN9/PIN10/PIN11 output

write Register 0x7B, [data]

[data] BIT vs output

Bit:

0	PIN9 1: Open Drain; 0:Output 0; Default 1
1	PIN10 1: Open Drain; 0:Output 0; Default 1
2	PIN11 1: Open Drain; 0:Output 0; Default 1
3	No use; Default 0
4	EN_G_12PIN 1: Open Drain; 0:Output 0; Default 0
5	EN_B_13PIN 1: Open Drain; 0:Output 0; Default 0
6	EN_R_14PIN 1: Open Drain; 0:Output 0; Default 0
7	LED Dimming enable ;1. PWM 9.7KHz output; 0: PWM Disable; Default :0

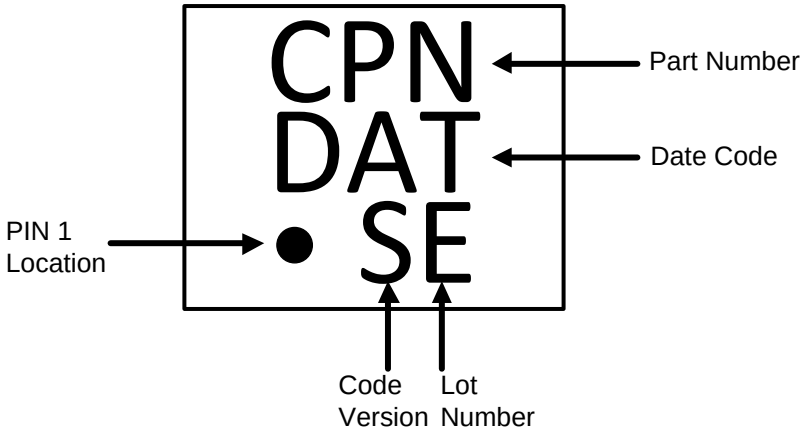
3. LED1/LED2/LED3 brightness control

Register Address

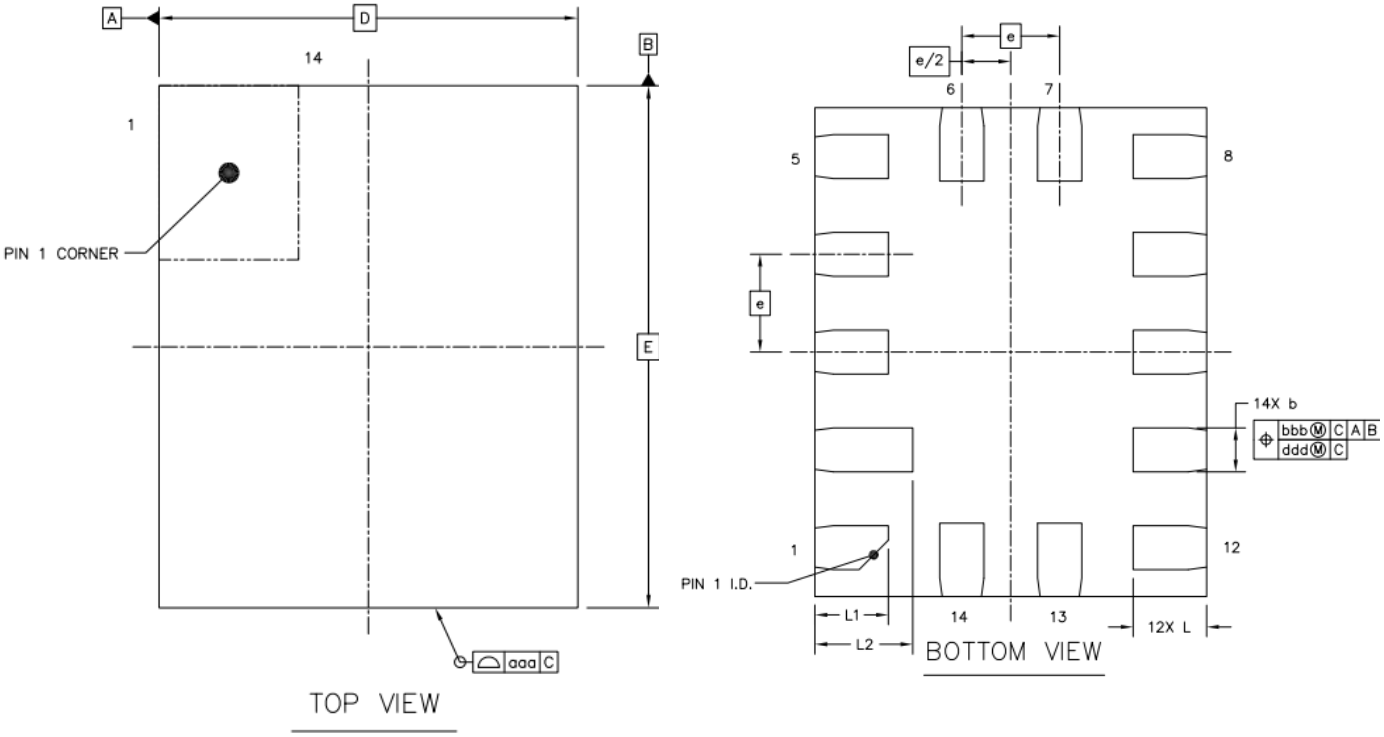
LED1: 0xCE; LED2: 0xCF; LED3: 0xD0

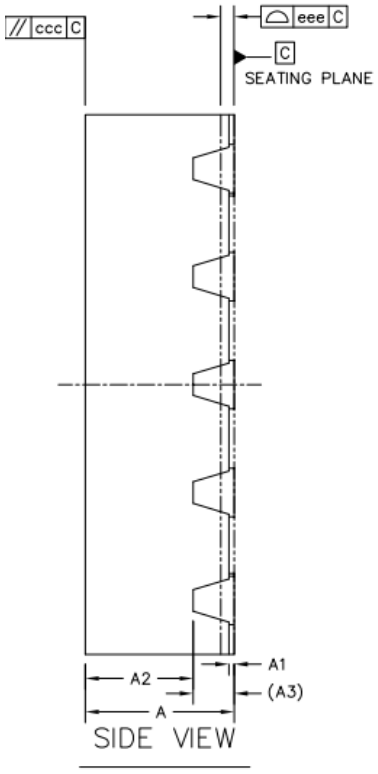
8bit register value is the PWM duty, from 0 to 100%

Package Top Marking



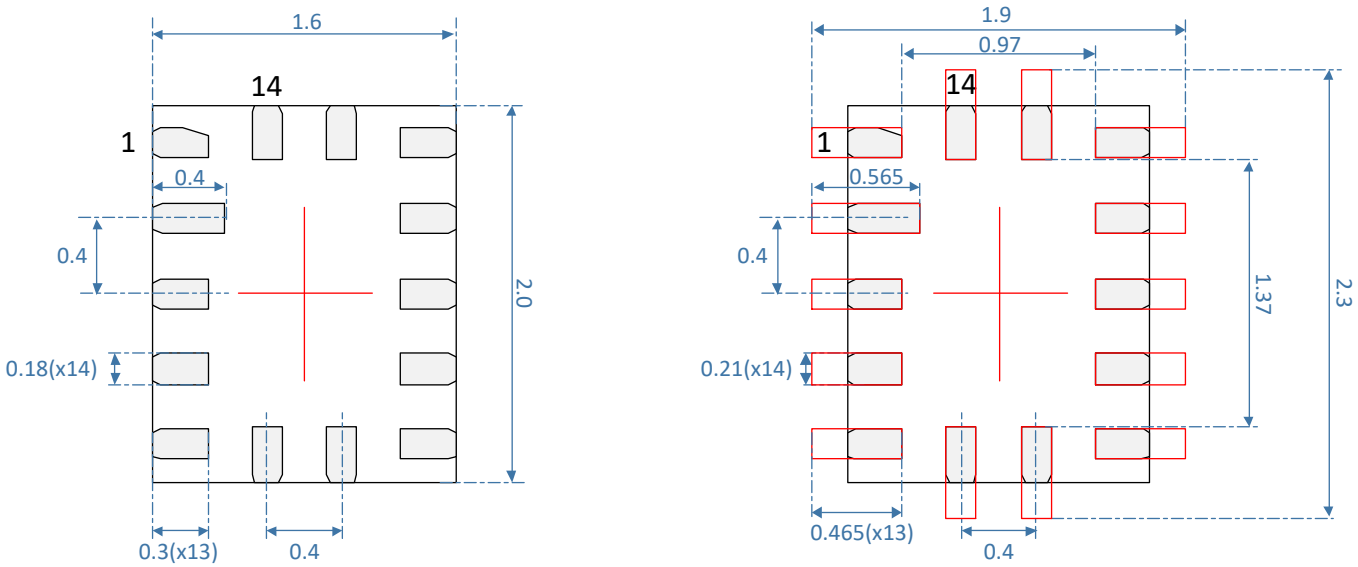
Package Drawing and Dimensions





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		1.6 BSC	
	Y	E		2 BSC	
LEAD PITCH		e		0.4 BSC	
LEAD LENGTH		L	0.25	0.3	0.35
		L1	0.2	0.3	0.4
		L2	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	

Recommended Land Pattern

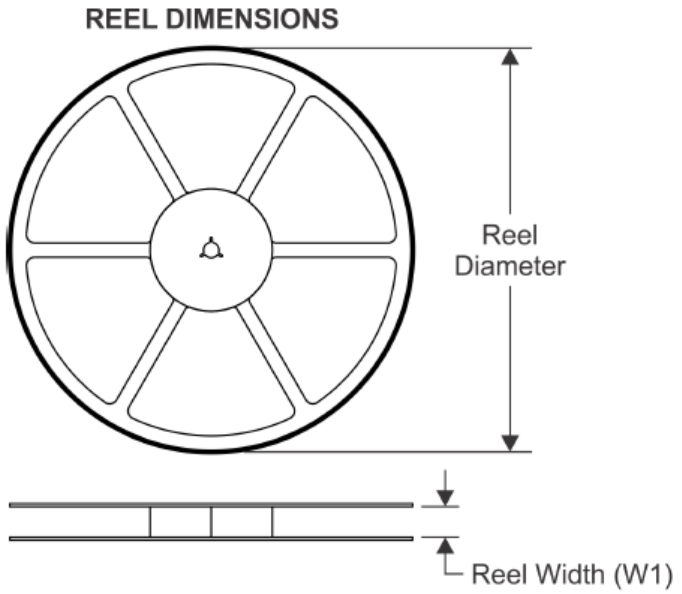


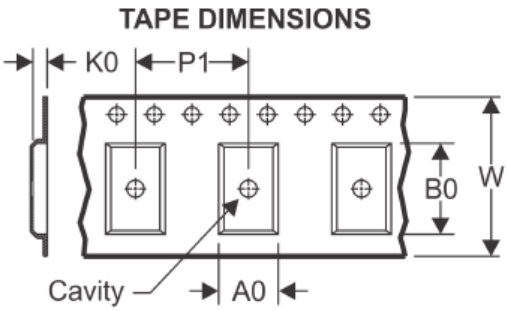
Unit: mm

Tape and Reel Information

Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
QFN 14L 1.6x2.0 mm	14	1.6x2.0x0.55	3000	3000	178/54	30	120	140	560	8	4

Carrier Tape Drawing and Dimensions





A0	Dimension designed to accommodate the component width	1.76mm
B0	Dimension designed to accommodate the component length	2.16mm
K0	Dimension designed to accommodate the component thickness	0.73mm
W	Overall width of the carrier tape	8.00mm
W1	Reel Width	9.50mm
P0	Pitch between Index Hole Pitch	4.00mm
P1	Pitch between successive cavity centers	4.00mm

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020