Product Introduction

LS98102 is a general and configurable analog digital hybrid chip, characterized by small size, ultra-low power consumption, and high reliability. Customers can design chips based on their own functional requirements, configure the connections between the simulation and logic functional macrocell inside LS98102, and burn the design into the internal NVM (Non-Volatile Memory). The internal functional blocks are as follows:

- One Multi-channel High Speed ACMP
- One Multi-channel Low Power ACMP
- One Voltage Reference Output
- One Differential/Single ended PGA
- Two DCMP/PWM
- Twenty Combination Function Macrocells
  - Four 2-bit LUT/DFF
  - Two 2-bit LUT/Pattern Generator
  - Two 2-bit LUT/Edge Detector
  - Ten 3-bit LUT/DFF
  - Two 3-bit LUT/Pipe Delay
- Twelve Multi-Function Blocks (MFB)
  - Ten Selectable 3-bit LUT/DFF + 8-bit Counter/Delay
  - One Selectable 4-bit LUT/DFF + 16-bit Counter/Delay
  - One 4-bit LUT/8-bit FSM CNT/DLY
- I^2C Protocol Interface
- Two Internal Oscillators
  - One 20Mhz & 2.5Mhz Oscillator
  - One 2Khz Oscillator
- Power-On Reset (POR)
- The Read Protection Function
- Wide Range Power Supply VDD: 2.3V to 5.5V
- Operating Temperature Range: -40℃ to 125℃
- RoHS Compliant/Halogen-Free
- Package: 14-L QFN: 3.0 x 3.0 x 0.75mm, 0.65mm pitch

Applications

- Automotive gateway, central control, instrument panel
- New Energy Transmission and Storage
- Motor Control
- Medical Equipment
- Security Products

Glossary

A

- ACMP: Analog Comparator
- ACMPH: Analog Comparator High Speed
- ACMPL: Analog Comparator Low Speed

B

- BG: Bandgap

C

- CLK: Clock
- CNT: Counter

D

- DFF: D Flip-Flop
- DLY: Delay
- DCMP: Digital Comparator

E

- ESD: Electrostatic discharge

F

- FSM: Finite State Machine

G

- GPI: General Purpose Input
- GPIO: General Purpose Input/Output
- GPO: General Purpose Output

I

- IN: Input
- IO: Input/Output

L

- LSB: Least Significant Bit
- LUT: Look-Up Table
- LV: Low Voltage

M

- MSB: Most Significant Bit
- MUX: Multiplexer
- MFB: Multi-Function Block

N

- nRST: Reset
- NVM: Non-Volatile Memory

O

- OE: Output Enable
- OSC: Oscillator
- OUT: Output

P

- PDWM: Power-down
- PGen: Pattern Generator
- POR: Power-On Reset
- PP: Push-Pull
- PGA: Programmable Gain Amplifier
- PWM: Pulse Width Modulator
- PDLY: Programmable Delay

S

- SCL: I^2C Clock Input
- SDA: I^2C Data Input/Output
- SLA: Slave Address
- SMT: With Schmitt Trigger

T

- TS: Temperature Sensor

V

- VREF: Voltage Reference

W

- WOSMT: Without Schmitt Trigger

Contents

1. System Block

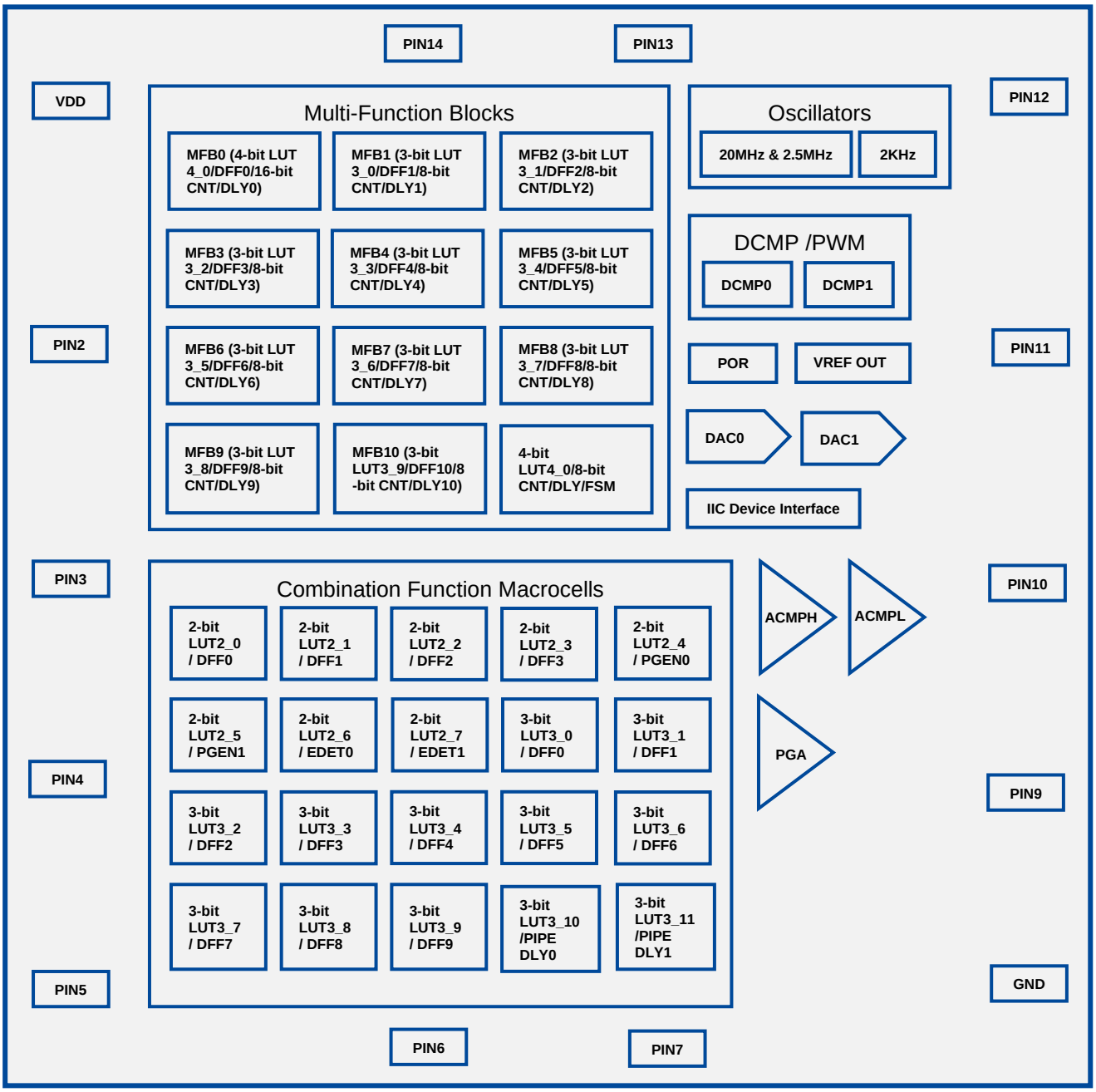


Figure 1: Block Diagram

2. Pin Definition

2.1 Pin Configuration-QFN-14L

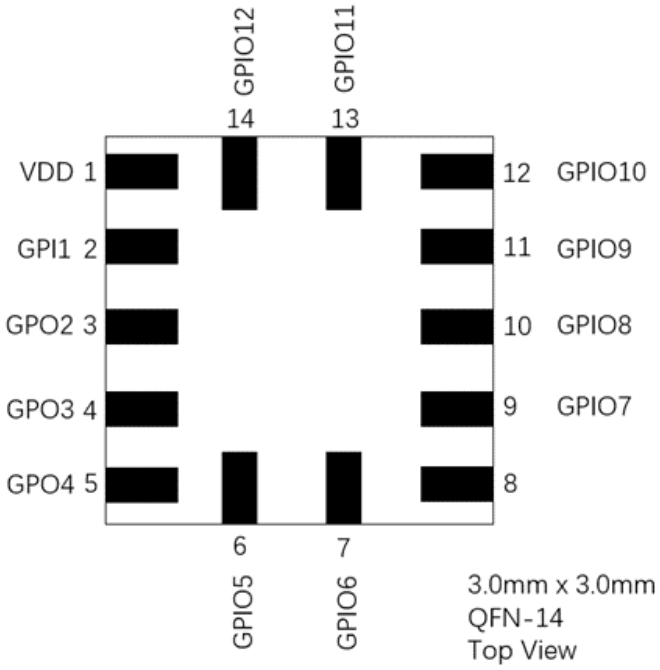


Figure 2：TQFN-14L (TOP View)

2.2 Pin Function Description

Table 1：Pin Function Description

Pin	Name	Type	Function
1	VDD	Power Source	VDD
2	GPI1	GPI	GPI, Digital Input
		SLA_0	I²C Slave address bit 0
		GPI	OSC0_EXT_CLK_IN, OSC0 External Clock Input
3	GPIO2	GPIO2	GPIO2, I²C_SCL
		I²C SCL	I²C_SCL
		ADC_VREF	ADC External Input Reference
		VREF0_OUT	VREF0 Output
4	GPIO3	GPIO3	GPIO3, I²C_SDA
		I²C SDA	I²C_SDA
		PGA _OUT	PGA Direct Output
5	GPIO4	GPIO with OE	GPIO with OE Control
		EXT_VREF0_IN	ACMP External Reference Source Input
		SLA_1	I²C Slave address bit 1
		OSC1_EXT_CLK_IN	OSC1 External Clock Input
6	GPIO5	GPIO with OE	GPIO Digital Input/Output IO with OE
		PGA+	PGA Input channel 1 or" +" terminal
7	GPIO6	GPIO with OE	GPIO with OE Control
		PGA-	PGA Input channel 2 or "-" terminal
		EXT_VREF1_IN	ACMP External Reference Source Input
8	GND	--	GND
9	GPIO7	GPIO with OE	GPIO with OE Control
		ACMP0_H+	ACMP0_H Positive Input
		SLA_2	I²C Slave address bit 2
10	GPIO8	GPIO with OE	GPIO with OE Control
		ACMP1_H+	ACMP1_H Positive Input
		SLA_3	I²C Slave address bit 3
11	GPIO9	GPIO with OE	GPIO with OE Control
		PGA_MUX	PGA MUX has internal matrix connections
		ACMP2_L+	ACMP2_L Positive Input
12	GPIO10	GPIO with OE	GPIO with OE Control
		ACMP3_L+	ACMP3_L Positive Input
13	GPIO11	GPIO with OE	GPIO with OE Control
		TS_OUT	Temperature Sensor Analog Output
		OSC2_EXT_CLK_IN	OSC2 External Reference Frequency Input
14	GPIO12	GPIO with OE	GPIO with OE Control
		VREF1_OUT	VREF1 Input

3. Characteristics

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Analog and digital grounds must be connected together on the PCB board. The place of connection depends on customers' schematic. For application cases with low digital current of LS98102, both AGND and GND should be connected to analog ground plane.

Table 2: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VDD to GND	-0.3	7	V
IO maximum voltage	-0.3	7	V
VDD to GND Maximum DC current	--	90	mA
Input leakage current	--	1000	nA
Storage temperature	-65	150	℃
Junction temperature	--	150	℃
Moisture Sensitivity Level (MSL)	1		--

3.2 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Min	Max	Unit
VDD Supply Voltage	2.3	5.5	V
Operating Temperature	-40	125	℃
Maximum voltage input to Pin	-0.2	VDD+0.3	V
Capacitor Value at VDD	0.1	--	uF

3.3 Electrostatic Discharge Ratings

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Charged Device Model)	500	--	V
ESD Protection (Human Body Model)	2000	--	V

3.4 Electrical Characteristics

Table 5：Electrical Characteristics (VDD: 2.5V±8%, Temp: -40~125°C)

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
POR						
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.67	1.80	1.92	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.77	1.25	1.54	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.50	--	ms
I_{stand_by}		T=+25 °C	--	70	--	nA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7*VDD	--	--	V
		Logic Input with Schmitt Trigger	0.8*VDD	--	--	V
		Low-Level Logic Input	0.75	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.3*VDD	V
		Logic Input with Schmitt Trigger	--	--	0.2*VDD	V
		Low-Level Logic Input	--	--	0.70	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.42	--	V
I_{LKG}	Input leakage (Absolute Value)	--	--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 1 mA, 1X Drive	2.013	--	--	V
		Push-Pull, I_{OH} = 1 mA, 2X Drive	2.09	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 1 mA, 1X Drive	--	--	0.12	V
		Push-Pull, I_{OL} = 1 mA, 2X Drive	--	--	0.07	V
		Open Drain, I_{OL} = 1 mA, 1X Drive	--	--	0.06	V
		Open Drain, I_{OL} = 1 mA, 2X Drive	--	--	0.055	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push-Pull,V_{OH} = VDD - 0.2,1X Drive	1.37	--	--	mA
		Push-Pull,V_{OH} = VDD - 0.2,2X Drive	2.74	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push-Pull, V_{OL} = 0.15 V, 1X Drive	1.61	--	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive	3.22	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Drive	4.9	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Drive	9.8	--	--	mA
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	KΩ
		10 k Pull Up	--	10	--	KΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	KΩ
		10 k Pull Down	--	10	--	KΩ
Oscillators						
Power-On time	20MHz OSC	T=+25 °C	--	0.453	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	19.73	--	MHz
		T=-40 °C to +125 °C	18.18	--	20.336	MHz
Power Consumption		T=+25 °C	--	60	--	uA
		T=-40 °C to +125 °C	--	--	117	uA
Power-On time	2.5MHz OSC	T=+25 °C	--	0.499	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	2.466	--	MHz
		T=-40 °C to +125 °C	2.27	--	2.542	MHz
Power Consumption		T=+25 °C	--	37	--	uA
		T=-40 °C to +125 °C	--	--	71.4	uA

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
Power-On time	2KHz OSC	T=+25 °C	--	600	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	2	--	KHz
		T=-40 °C to +125 °C	1.726	--	2.074	KHz
Power Consumption		T=+25 °C	--	0.41	--	uA
		T=-40 °C to +125 °C	--	--	1.68	uA
ACMPH Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1.23	V
V_{offset}	ACMP Input Offset	--	-5	2	5	mV
Input Buffer	Bandwidth		--	500	--	KHz
	Offset		-9.6	4.8	9.6	mV
	Power Consumption		--	1.5	--	uA
t_{start}	ACMP Startup Time when BG On	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxH	--	33	--	uS
	ACMP Startup Time when BG Off		--	1	--	mS
R_{sin}	Series Input Resistance	Gain = 1	--	1	--	GΩ
		Gain = 1/2	1.2	1.34	1.48	MΩ
		Gain = 1/4	1.2	1.34	1.48	MΩ
		Gain = 1/5	1.2	1.34	1.48	MΩ
PROP	Propagation Delay, Response Time	Overdrive = 50 mV	--	0.366	0.492	uS
G	Gain	G=1	--	1	--	
		G=1/2 (ACMP- = 0.6V)	0.4969	0.5	0.5031	
		G=1/4 (ACMP- = 0.75V)	--	--	--	
		G=1/5 (ACMP- = 1.1V)	--	--	--	
Vref	Internal Vref error, Vref=0 to1.23V	T=+25 °C	--	5	--	mV
		T=-40 °C to +125 °C	-1.7%	--	1.7%	Fs
Power Consumption		Internal Vref Without Input Buffer	--	9.0	--	uA
ACMPL Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1.23	V
V_{offset}	ACMP Input Offset	--	-5	2	5	mV
t_{start}	ACMP Startup Time when BG ON	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL	--	78	--	uS
	ACMP Startup Time when BG Off		--	1	--	mS
R_{sin}	Series Input Resistance	Gain = 1	--	1	--	GΩ
		Gain = 1/2	1.2	1.34	1.48	MΩ
		Gain = 1/4	1.2	1.34	1.48	MΩ
		Gain = 1/5	1.2	1.34	1.48	MΩ
PROP	Propagation Delay, Response Time	Overdrive = 50 mV	--	5.926	8.447	uS
G	Gain	G=1	--	1	--	
		G=1/2 (ACMP- = 0.6V)	0.4973	0.5	0.5027	
		G=1/4 (ACMP- = 0.75V)	--	--	--	
		G=1/5 (ACMP- = 1.1V)	--	--	--	
Vref	Internal Vref error, Vref=0 to1.23V	T=+25 °C	--	5	--	mV
		T=-40 °C to +125 °C	-1.7%	--	1.7%	Fs
Power Consumption		Internal Vref	--	3.8	--	uA

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
Vref Out Characteristics						
$Vref_{Accuracy}$	Vref Gain Accuracy	G=1	--	1	--	
		G=2	-0.501%	2	0.484%	
$Vref_{offset}$	Vref Opamp Offset	G=1 (VCM IN=VDD/2)	-6	3	6	mV
Vref DAC_{offset}			-1.7%	0.5%	1.7%	Fs
$I_{loading}$		Source Current	--	2	--	mA
Power Consumption		G=1	--	1.77	--	uA
Turn On Time		0.5% Accuracy	--	150	--	uS
Voltage of Output to VDD		Maximum output voltage $\mathrm{Vout} = \mathrm{VDD} - 0.3 - 300\Omega \times \mathrm{Iout}$				
PGA						
Input Range			0	--	VDD	V
Linear Output Range			0.1	--	VDD-0.1	V
V_{offset}	Single End	G=1(+25 °C)	--	1.5	6.5	mV
		G=1(-40 °C to +125 °C)	--	--	8	mV
	Differential	G=1(+25 °C)	--	3	13.5	mV
		G=1(-40 °C to +125 °C)	--	--	19.5	mV
Gain Error	Single End	G=1	--	1	--	
		G=2	-2.2%	2	2.2%	
		G=4	-3.5%	4	3.5%	
		G=8	-3.1%	8	3.1%	
		G=16	-2.7%	16	2.7%	
	Differential	G=1	--	1	--	
		G=2	-2.3%	2	2.3%	
		G=4	-2.4%	4	2.4%	
		G=8	-2.0%	8	2.0%	
		G=16	-2.3%	16	2.3%	
Bandwidth		G=1	--	700	--	KHz
Turn On Time		0.5% Accuracy	--	20	--	uS
Power Consumption	Single End		--	38	--	uA
	Differential		--	129	--	uA
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

Table 6：Electrical Characteristics (VDD: 3.3V±10%, Temp: -40~125°C)

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
POR						
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.67	1.80	1.92	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.77	1.25	1.54	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.50	--	ms
I_{stand_by}		T=+25 °C	--	97	--	nA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7*VDD	--	--	V
		Logic Input with Schmitt Trigger	0.8*VDD	--	--	V
		Low-Level Logic Input	0.82	--	--	V

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.3*VDD	V
		Logic Input with Schmitt Trigger	--	--	0.2*VDD	V
		Low-Level Logic Input	--	--	0.77	V
V_{HYS}	SchmittTrigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.45	--	V
I_{LKG}	Input leakage (Absolute Value)	--	--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 3 mA, 1X Drive	2.56	--	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive	2.71	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 3 mA, 1X Drive	--	--	0.3	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive	--	--	0.18	V
		Open Drain, I_{OL} = 3 mA, 1X Drive	--	--	0.15	V
		Open Drain, I_{OL} = 3 mA, 2X Drive	--	--	0.1	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push-Pull, V_{OH} = 2.4 V , 1X Drive	5	--	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive	10	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push-Pull, V_{OL} = 0.4 V, 1X Drive	5	--	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	10	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	15	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	30	--	--	mA
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	KΩ
		10 k Pull Up	--	10	--	KΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	KΩ
		10 k Pull Down	--	10	--	KΩ
Oscillators						
Power-On time	20MHz OSC	T=+25 °C	--	0.445	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	19.90	--	MHz
		T=-40 °C to +125 °C	18.34	--	20.504	MHz
Power Consumption		T=+25 °C	--	73	--	uA
		T=-40 °C to +125 °C	--	--	114.6	uA
Power-On time	2.5MHz OSC	T=+25 °C	--	0.472	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	2.488	--	MHz
		T=-40 °C to +125 °C	2.29	--	2.563	MHz
Power Consumption		T=+25 °C	--	40	--	uA
		T=-40 °C to +125 °C	--	--	79.6	uA
Power-On time	2KHz OSC	T=+25 °C	--	569	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	2	--	KHz
		T=-40 °C to +125 °C	1.724	--	2.072	KHz
Power Consumption		T=+25 °C	--	0.44	--	uA
		T=-40 °C to +125 °C	--	--	1.85	uA
ACMPH Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1.23	V
V_{offset}	ACMP Input Offset	--	-5	2	5	mV
Input Buffer	Bandwidth		--	500	--	KHz
	Offset		-9.6	4.8	9.6	mV
	Power Consumption		--	2	--	

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
t_{start}	ACMP Startup Time when BG ON	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxH	--	29	--	uS
	ACMP Startup Time when BG Off		--	1	--	mS
R_{sin}	Series Input Resistance	Gain = 1	--	1	--	GΩ
		Gain = 1/2	1.2	1.34	1.48	MΩ
		Gain = 1/4	1.2	1.34	1.48	MΩ
		Gain = 1/5	1.2	1.34	1.48	MΩ
PROP	Propagation Delay, Response Time	Overdrive = 50 mV	--	0.338	0.423	uS
G	Gain	G=1	--	1	--	
		G=1/2 (ACMP- = 0.6V)	0.4970	0.5	0.5030	
		G=1/4 (ACMP- = 0.75V)	0.2475	0.25	0.2525	
		G=1/5 (ACMP- = 1.1V)	--	--	--	
Vref	Internal Vref error, Vref=0 to1.23V	T=+25 °C	--	5	--	mV
		T=-40 °C to +125 °C	-1.7%	--	1.7%	Fs
Power Consumption		Internal Vref Without Input Buffer	--	9.3	--	uA
ACMPL Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1.23	V
V_{offset}	ACMP Input Offset	--	-5	2	5	mV
t_{start}	ACMP Startup Time when BG ON	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL	--	75	--	uS
	ACMP Startup Time when BG Off		--	1	--	mS
R_{sin}	Series Input Resistance	Gain = 1	--	1	--	GΩ
		Gain = 1/2	1.2	1.34	1.48	MΩ
		Gain = 1/4	1.2	1.34	1.48	MΩ
		Gain = 1/5	1.2	1.34	1.48	MΩ
PROP	Propagation Delay, Response Time	Overdrive = 50 mV	--	6.115	8.596	uS
G	Gain	G=1	--	1	--	
		G=1/2 (ACMP- = 0.6V)	0.4971	0.5	0.5029	
		G=1/4 (ACMP- = 0.75V)	0.2472	0.25	0.2528	
		G=1/5 (ACMP- = 1.1V)	--	--	--	
Vref	Internal Vref error, Vref=0 to1.23V	T=+25 °C	--	5	--	mV
		T=-40 °C to +125 °C	-1.7%	--	1.7%	Fs
Power Consumption		Internal Vref	--	3.9	--	uA
Vref Out Characteristics						
$Vref_{Accuracy}$	Vref Gain Accuracy	G=1	--	1	--	
		G=2	-0.538%	2	0.439%	
$Vref_{offset}$	Vref Opamp Offset	G=1 (VCM IN=VDD/2)	-6	3	6	mV
Vref DAC_{offset}			-1.7%	0.5%	1.7%	Fs
$I_{loading}$		Source Current	--	2	--	mA
Power Consumption		G=1		1.86	--	uA
Turn On Time		0.5% Accuracy	--	150	--	uS
Voltage of Output to VDD		Maximum output voltage $\mathrm{Vout} = \mathrm{VDD} - 0.3 - 300\Omega \times \mathrm{Iout}$				

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
PGA						
Input Range			0	--	VDD	V
Linear Output Range			0.1	--	VDD-0.1	V
V_{offset}	Single End	G=1(+25 °C)	--	1.5	6.5	mV
		G=1(-40 °C to +125 °C)	--	--	8	mV
	Differential	G=1(+25 °C)	--	3	14.5	mV
		G=1(-40 °C to +125 °C)	--	--	21	mV
Gain Error	Single End	G=1	--	1	--	
		G=2	-2.2%	2	2.2%	
		G=4	-3.5%	4	3.5%	
		G=8	-3.1%	8	3.1%	
		G=16	-2.7%	16	2.7%	
	Differential	G=1	--	1	--	
		G=2	-2.3%	2	2.3%	
		G=4	-2.4%	4	2.4%	
		G=8	-2.0%	8	2.0%	
		G=16	-2.3%	16	2.3%	
Bandwidth		G=1	--	700	--	KHz
Turn On Time		0.5% Accuracy	--	20	--	uS
Power Consumption		Single End	--	39	--	uA
		Differential	--	131	--	uA
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

Table 7：Electrical Characteristics (VDD: 5V±10%, Temp: -40~125°C)

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
POR						
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.67	1.80	1.92	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.77	1.25	1.54	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.50	--	ms
I_{stand_by}		T=+25 °C	--	155	--	nA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7*VDD	--	--	V
		Logic Input with Schmitt Trigger	0.8*VDD	--	--	V
		Low-Level Logic Input	0.94	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.3*VDD	V
		Logic Input with Schmitt Trigger	--	--	0.2*VDD	V
		Low-Level Logic Input	--	--	0.86	V
V_{HYS}	SchmittTrigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.54	--	V
I_{LKG}	Input leakage (Absolute Value)	--	--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 5 mA, 1X Drive	4.0	--	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Drive	4.17	--	--	V

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 5 mA, 1X Drive	--	--	0.34	V
		Push-Pull, I_{OL} = 5 mA, 2X Drive	--	--	0.22	V
		Open Drain, I_{OL} = 5 mA, 1X Drive	--	--	0.29	V
		Open Drain, I_{OL} = 5 mA, 2X Drive	--	--	0.14	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push-Pull, V_{OH} = 2.4 V , 1X Drive	19	--	--	mA
		Push-Pull, V_{OH} = 2.4 V , 2X Drive	38	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push-Pull, V_{OL} = 0.4 V, 1X Drive	7	--	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	14	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	21	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	42	--	--	mA
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	KΩ
		10 k Pull Up	--	10	--	KΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	KΩ
		10 k Pull Down	--	10	--	KΩ
Oscillators						
Power-On time	20MHz OSC	T=+25 °C	--	0.433	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	20.13	--	MHz
		T=-40 °C to +125 °C	18.52	--	20.776	MHz
Power Consumption		T=+25 °C	--	104	--	uA
		T=-40 °C to +125 °C	--	--	208	uA
Power-On time	2.5MHz OSC	T=+25 °C	--	0.445	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	2.516	--	MHz
		T=-40 °C to +125 °C	2.32	--	2.597	MHz
Power Consumption		T=+25 °C	--	48	--	uA
		T=-40 °C to +125 °C	--	--	98.4	uA
Power-On time	2KHz OSC	T=+25 °C	--	537	--	uS
Frequency		T=+25 °C	--	2	--	KHz
		T=-40 °C to +125 °C	1.722	--	2.071	KHz
Power Consumption		T=+25 °C	--	0.54	--	uA
		T=-40 °C to +125 °C	--	--	2.28	uA
ACMPH Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1.23	V
V_{offset}	ACMP Input Offset	--	-5	2	5	mV
Input Buffer	Bandwidth		--	500	--	KHz
	Offset		-9.6	4.8	9.6	mV
	Power Consumption		--	2	--	
t_{start}	ACMP Startup Time when BG ON	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxH	--	29	--	uS
	ACMP Startup Time when BG Off		--	1	--	mS
R_{sin}	Series Input Resistance	Gain = 1	--	1	--	GΩ
		Gain = 1/2	1.2	1.34	1.48	MΩ
		Gain = 1/4	1.2	1.34	1.48	MΩ
		Gain = 1/5	1.2	1.34	1.48	MΩ

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
PROP	Propagation Delay, Response Time	Overdrive = 50 mV	--	0.318	0.402	uS
G	Gain	G=1	--	1	--	
		G=1/2 (ACMP- = 0.6V)	0.4943	0.5	0.5057	
		G=1/4 (ACMP- = 0.75V)	0.2470	0.25	0.2530	
		G=1/5 (ACMP- = 1.1V)	0.1980	0.2	0.2019	
Vref	Internal Vref error, Vref=0 to1.23V	T=+25 °C	--	5	--	mV
		T=-40 °C to +125 °C	-1.7%	--	1.7%	Fs
Power Consumption		Internal Vref Without Input Buffer	--	10	--	uA
ACMPL Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0		1.23	V
V_{offset}	ACMP Input Offset	--	-5	2	5	mV
t_{start}	ACMP Startup Time when BG ON	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL	--	108	--	uS
	ACMP Startup Time when BG Off		--	1	--	mS
R_{sin}	Series Input Resistance	Gain = 1	--	1	--	GΩ
		Gain = 1/2	1.2	1.34	1.48	MΩ
		Gain = 1/4	1.2	1.34	1.48	MΩ
		Gain = 1/5	1.2	1.34	1.48	MΩ
PROP	Propagation Delay, Response Time	Overdrive = 50 mV	--	6.477	8.159	uS
G	Gain	G=1	--	1	--	
		G=1/2 (ACMP- = 0.6V)	0.4968	0.5	0.5032	
		G=1/4 (ACMP- = 0.75V)	0.2470	0.25	0.2529	
		G=1/5 (ACMP- = 1.1V)	0.1975	0.2	0.2025	
Vref	Internal Vref error, Vref=0 to1.23V	T=+25 °C	--	5	--	mV
		T=-40 °C to +125 °C	-1.7%	--	1.7%	Fs
Power Consumption		Internal Vref	--	4.2	--	uA
Vref Out Characteristics						
$Vref_{Accuracy}$	Vref Gain Accuracy	G=1	--	1	--	
		G=2	-0.597%	2	0.413%	
$Vref_{offset}$	Vref Opamp Offset	G=1 (VCM IN=VDD/2)	-6	3	6	mV
Vref DAC_{offset}			-1.7%	0.5%	1.7%	Fs
$I_{loading}$		Source Current	--	2	--	mA
Power Consumption		G=1	--	2.15	--	uA
Turn On Time		0.5% Accuracy	--	150	--	uS
Voltage of Output to VDD		Maximum output voltage $\mathrm{Vout} = \mathrm{VDD} - 0.3 - 300\Omega \times \mathrm{Iout}$				
PGA						
Input Range			0	--	VDD	V
Linear Output Range			0.1	--	VDD-0.1	V
V_{offset}	Single End	G=1(+25 °C)	--	1.5	8	mV
		G=1(-40 °C to +125 °C)	--	--	8	mV
	Differential	G=1(+25 °C)	--	3.5	15	mV
		G=1(-40 °C to +125 °C)	--	--	23.5	mV

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
Gain Error	Single End	G=1	--	1	--	
		G=2	-2.2%	2	2.2%	
		G=4	-3.5%	4	3.5%	
		G=8	-3.1%	8	3.1%	
		G=16	-2.7%	16	2.7%	
	Differential	G=1	--	1	--	
		G=2	-2.3%	2	2.3%	
		G=4	-2.4%	4	2.4%	
		G=8	-2.0%	8	2.0%	
		G=16	-2.3%	16	2.3%	
Bandwidth		G=1	--	700	--	KHz
Turn On Time		0.5% Accuracy	--	20	--	uS
Power Consumption		Single End	--	42	--	uA
		Differential	--	137	--	uA
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

Table 8：I²C Timing Parameter,（VDD: 2.3V ~ 5.5V, Temp: -40℃ ~ 125℃）

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	--	1000	KHz
t_{LOW}	Clock Pulse Width Low		1300	--	500	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	260	--	ns
t_I	Input Filter Spike Suppression (SCL,SDA)	VDD=2.5V±8%	--	95	--	168	ns
		VDD=3.3V±10%	--	95	--	157	ns
		VDD=5.0V±10%	--	111	--	156	ns
t_{AA}	Clock Low to Data Out Valid		--	900	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	500	--	ns
t_{HD_STA}	Start Hold Time		600	--	260	--	ns
t_{SU_STA}	Start Set-up Time		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time		0	--	0	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
t_R	Inputs Fail Time		--	300	--	120	ns
t_F	Inputs Rise Time		--	300	--	120	ns
t_{SU_STO}	Stop Set-up Time		600	--	260	--	ns
t_{DH}	Data out Hold Time		50	--	50	--	ns
Note: Timing Diagram can be found in the Figure 20.							

4. IO Pins

The LS98102 has a total of 11 GPIO Pins which can function as either a user-defined Input or Output, as well as serve as a special function (such as outputting the voltage reference) and 1 GPI Pin.

4.1 GPI Pin

GPI_1 serve as General Purpose Input Pin, it's internal block diagram is shown in Figure 3.

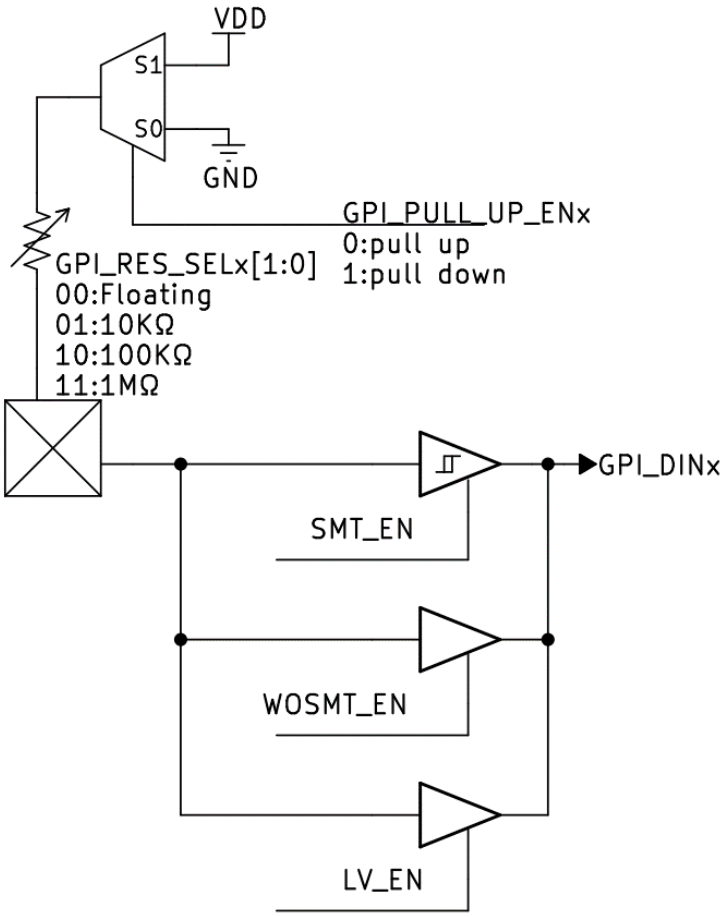


Figure 3：GPI_1 Structure Diagram

4.2 GPIO Pins

IO2、IO3、IO4、IO5、IO6、IO7、IO8、IO9、IO10、IO11 and IO12 serve as General Purpose IO Pins.

For the GPIO2(PIN3) and GPIO3(PIN4), which are applied to I²C-SCL and I²C-SDA, the system block diagram is shown in Figure 4.

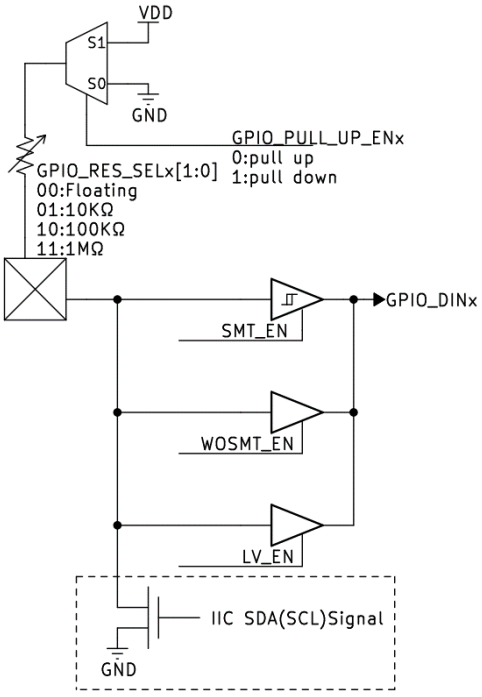


Figure 4：IO with I²C Mode IO Structure Diagram

For the IO4,5,6,7,8,9,10,11and IO12, the system block diagram is shown in Figure 5.

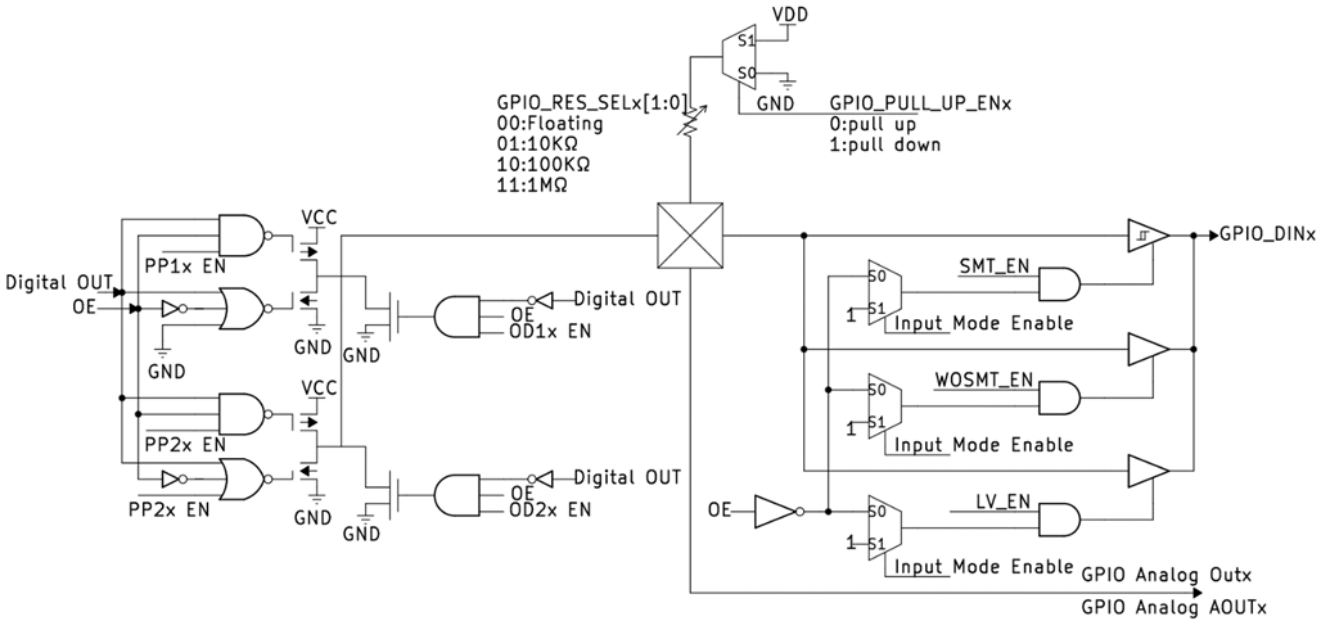


Figure 5：GPIO with OE Structure Diagram

5. Connection Matrix

LS98102 has three interconnected matrices internally, including one main matrix and two sub matrices. Through register configuration, the interconnection matrix can be used for internal resource connections as well as connections between the main matrix and sub matrices. These registers can be burned through OTP.

The input of the connection matrix comes from internal resources or the output of the connection matrix, while the output of the connection matrix is the input of internal resources or the connection matrix. The output of each connection matrix is configured through a set of registers.

6. Combination Function Macrocells

The LS98102 has twenty combination function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells:

- Four 2-bit LUT/DFF
- Two 2-bit LUT/Pattern Generator
- Two 2-bit LUT/Edge Detector
- Ten 3-bit LUT/DFF with nRST/nSET
- Two 3-bit LUT/Pipe Delay

6.1 2-bit LUT/DFF

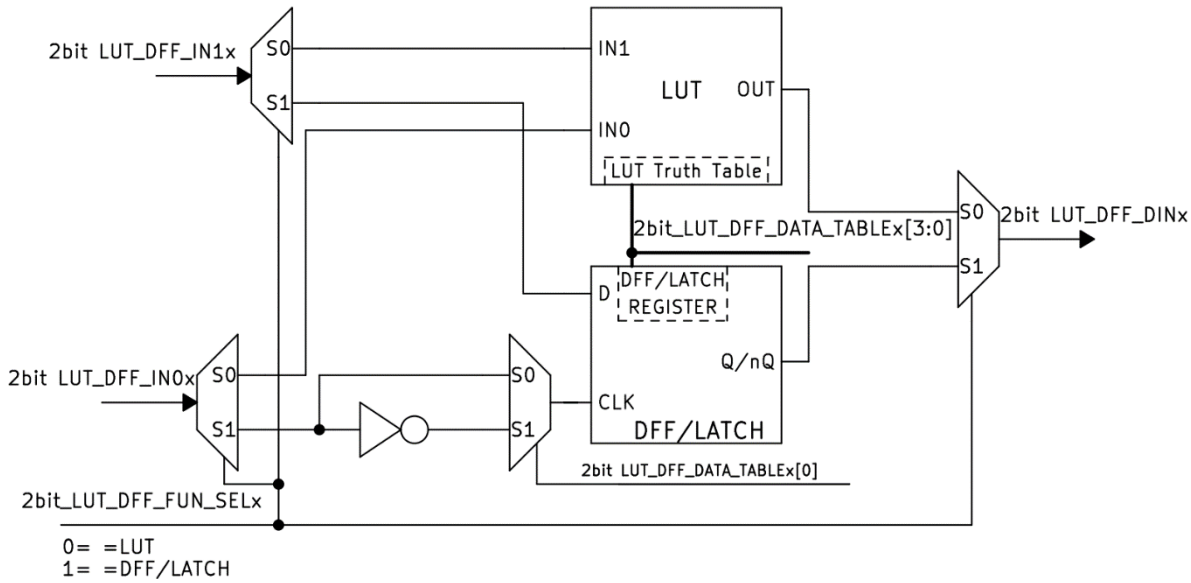


Figure 6：2-bit LUT/DFF

6.2 2-bit LUT/Pattern Generator

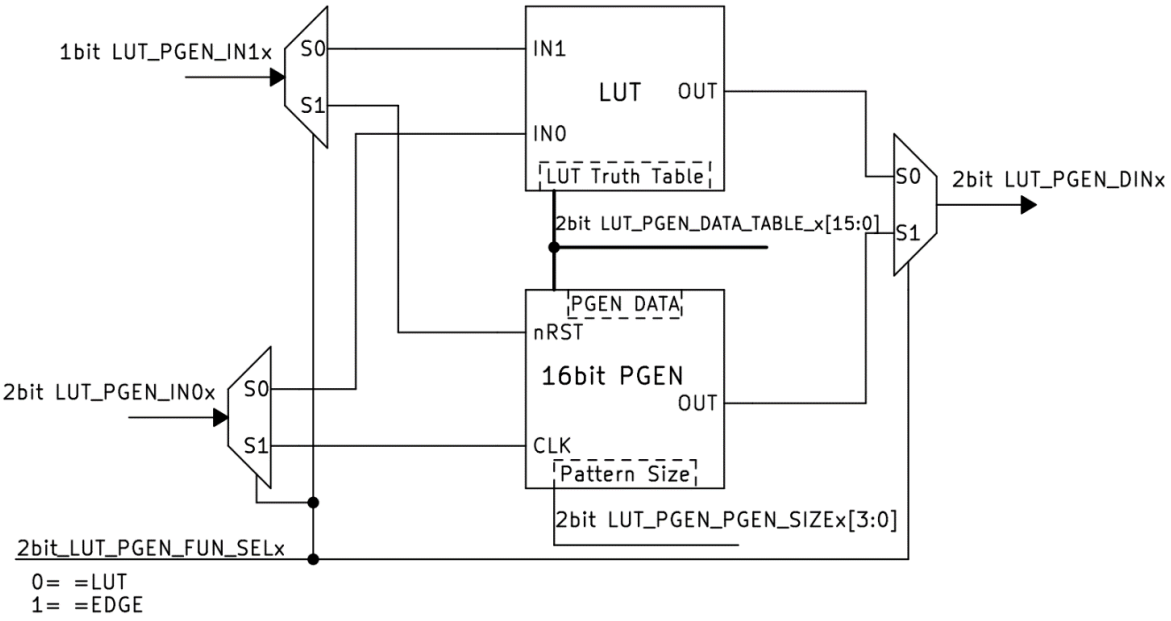


Figure 7：2-bit LUT/Pattern Generator

6.3 2-bit LUT/Edge Detector

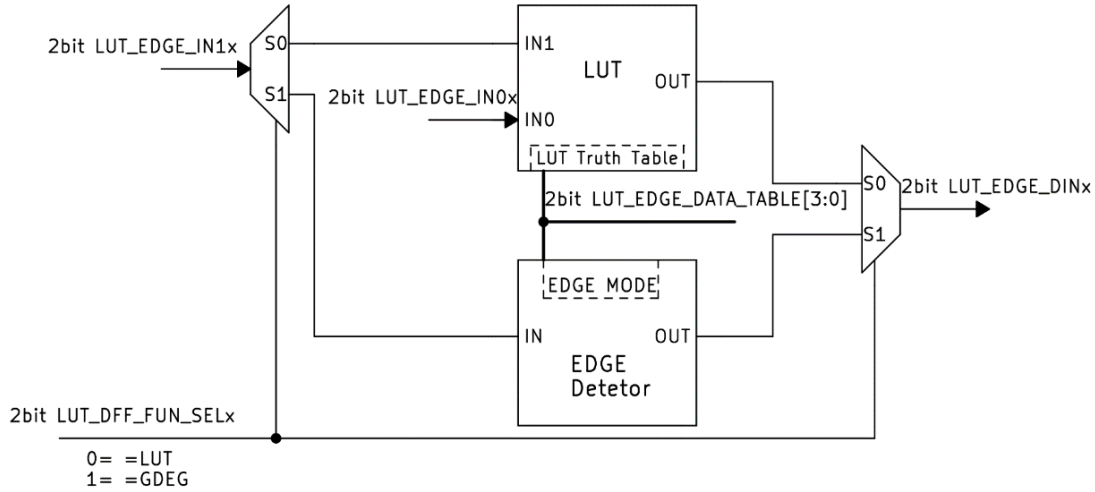


Figure 8：2-bit LUT/Edge Detector

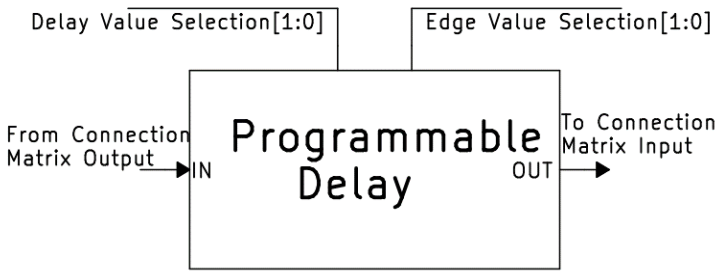


Figure 9：Programmable Delay

6.4 3-bit LUT/DFF with nRST/nSET

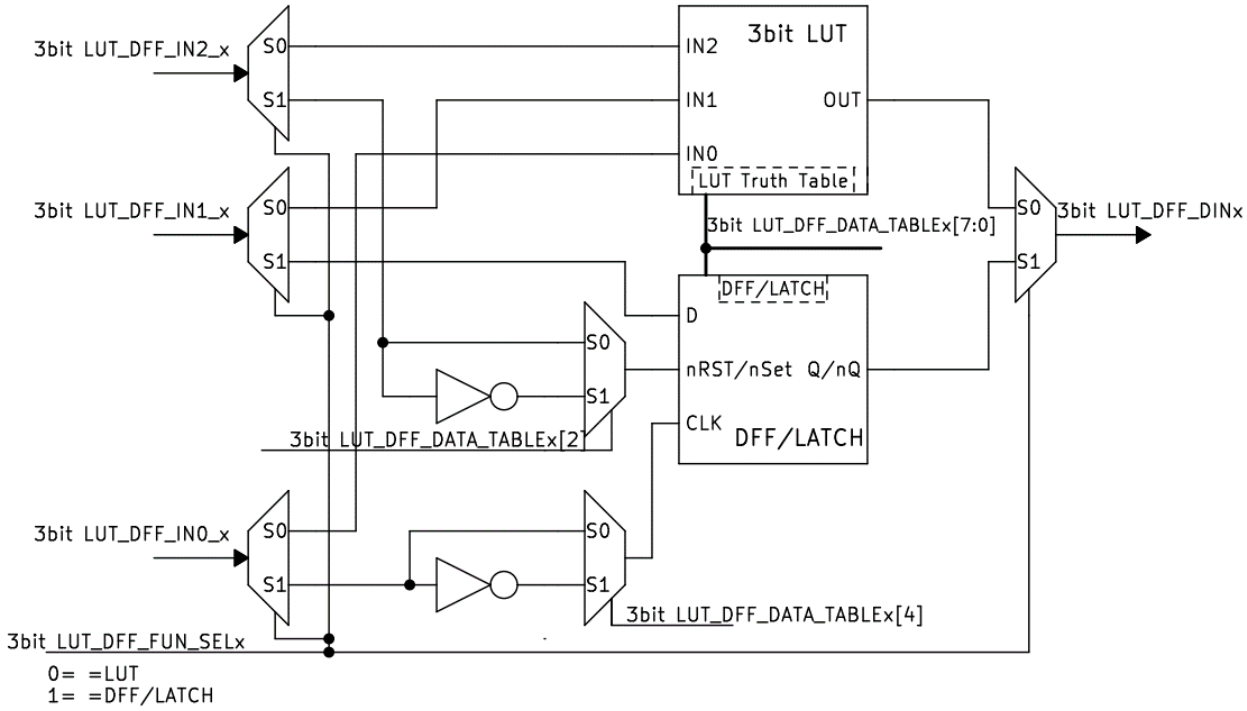


Figure 10：3-bit LUT/DFF

6.5 3-bit LUT/Pipe Delay

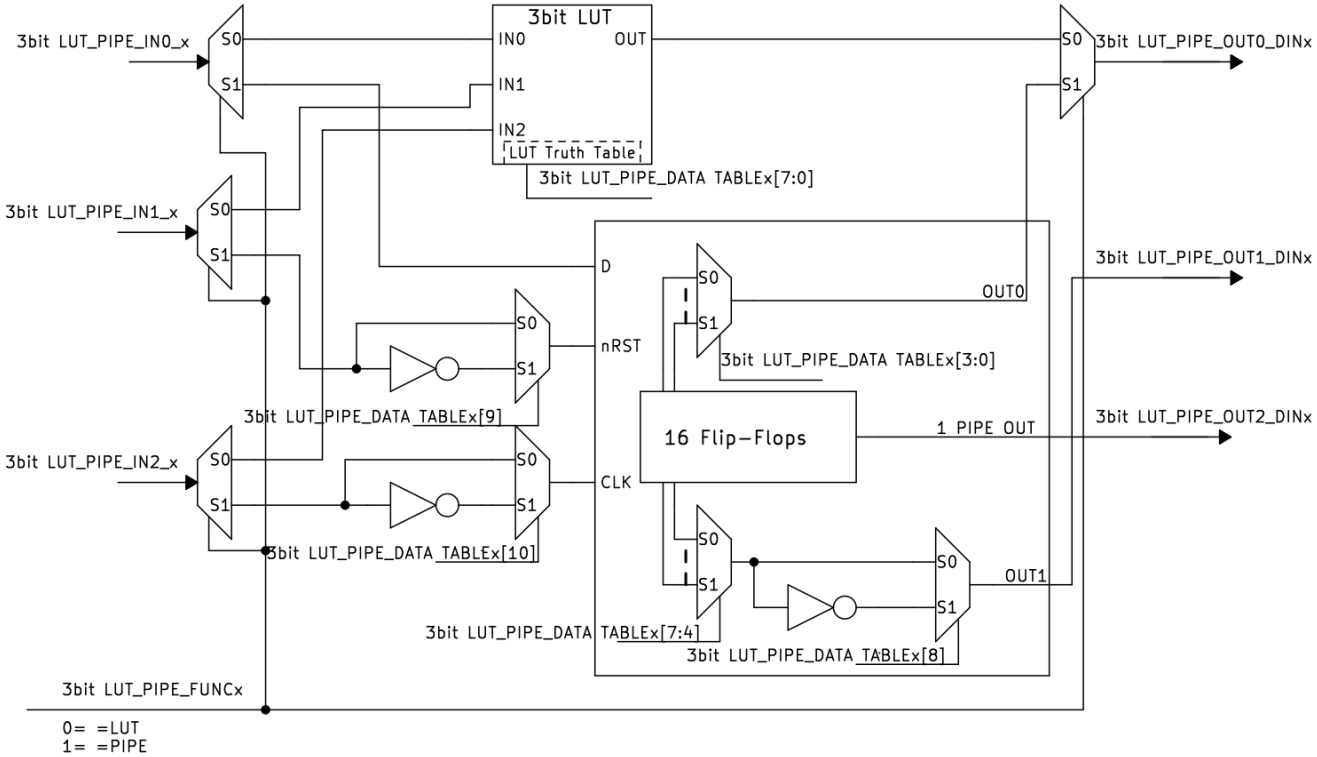


Figure 11：3-bit LUT/Pipe Delay

7. Multi-Function Block（MFB）

LS98102 has eleven Multi-Function Blocks that can serve as more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes s such as One Shot, Frequency Detect, Edge Detect, and others.

Also, the block is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF.

The LS98102 also has one FSM Counter that can be individually set to 4-bit LUT or 8-bit FSM CNT/DLY.

See the list below for the functions that can be implemented in these blocks:

- Ten Selectable 3-bit LUT/DFF + 8-bit Counter/Delay
- One Selectable 4-bit LUT/DFF + 16-bit Counter/Delay
- One 4-bit LUT/8-bit FSM CNT/DLY

7.1 3-bit LUT/DFF or 8-bit Counter/Delay Block Diagram

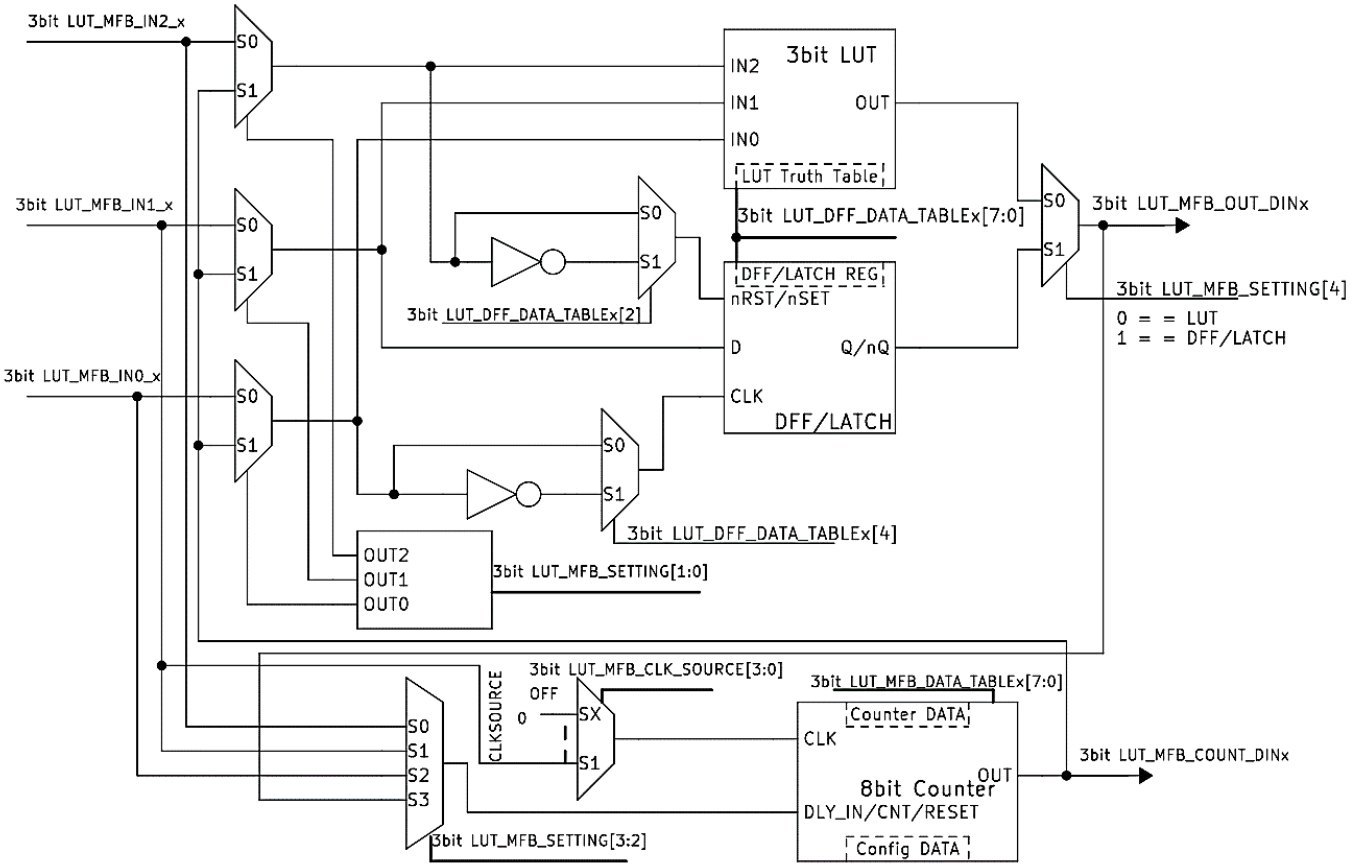


Figure 12：3-bit LUT or 8-bit Counter/Delay

7.2 4-bit LUT/DFF or 16-bit Counter/Delay Block Diagram

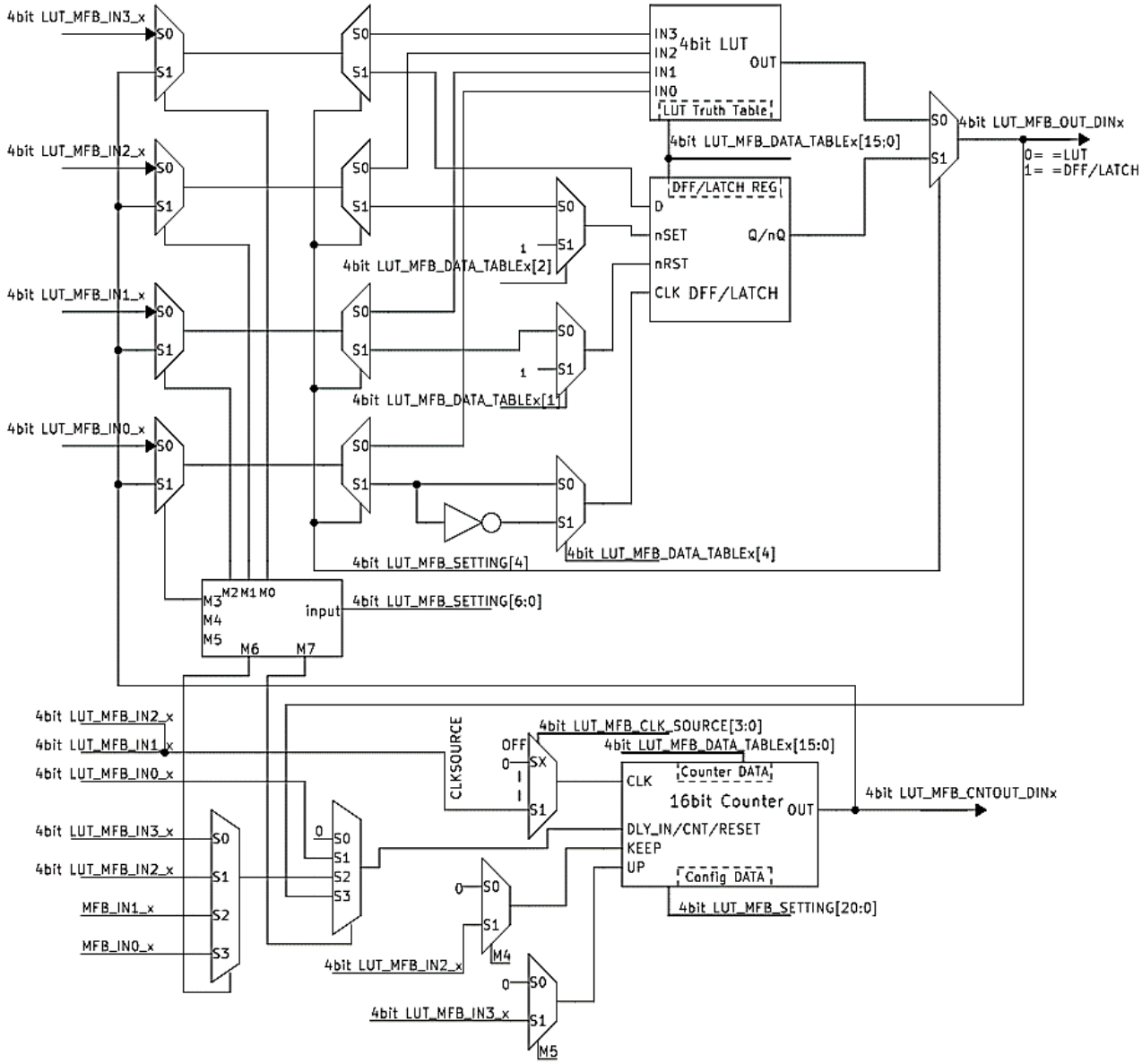


Figure 13：4-bit LUT or 16-bit Counter/Delay

7.3 4-bit LUT/8-bit FSM CNT/DLY Block Diagram

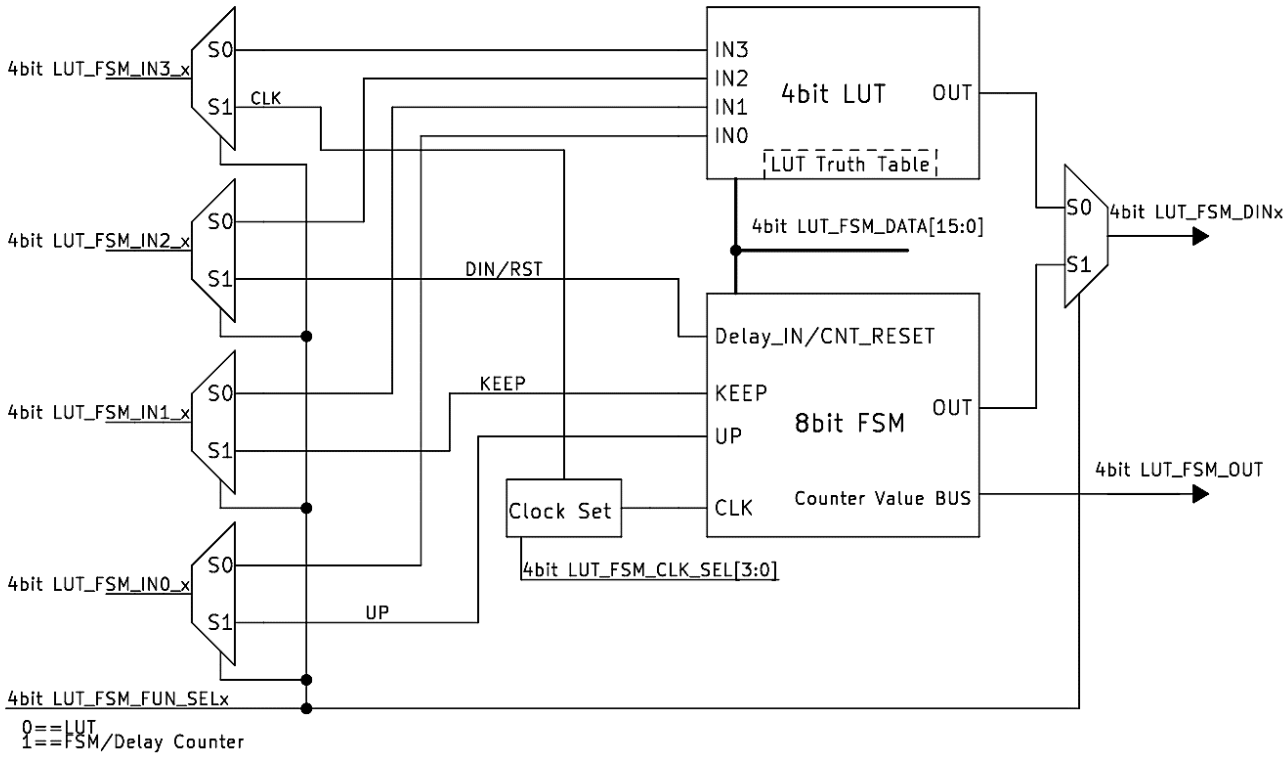


Figure 14：4-bit LUT or 8-bit FSM

8. I²C Communication Interface

The LS98102 provides an I²C communication interface that allows the I²C master to read or write internal registers, thereby remotely reconfiguring internal resources and their connection relationships.

8.1 I²C Read

8.1.1 Current Address Read Command

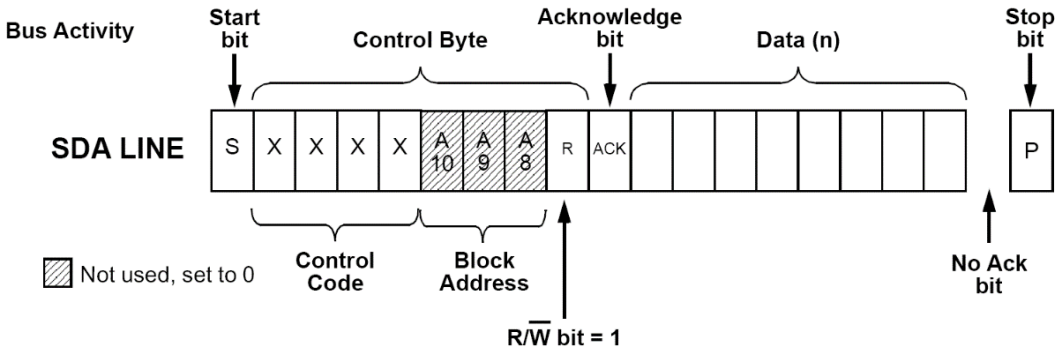


Figure 15：Current Address Read Command

8.1.2 Random Read Command

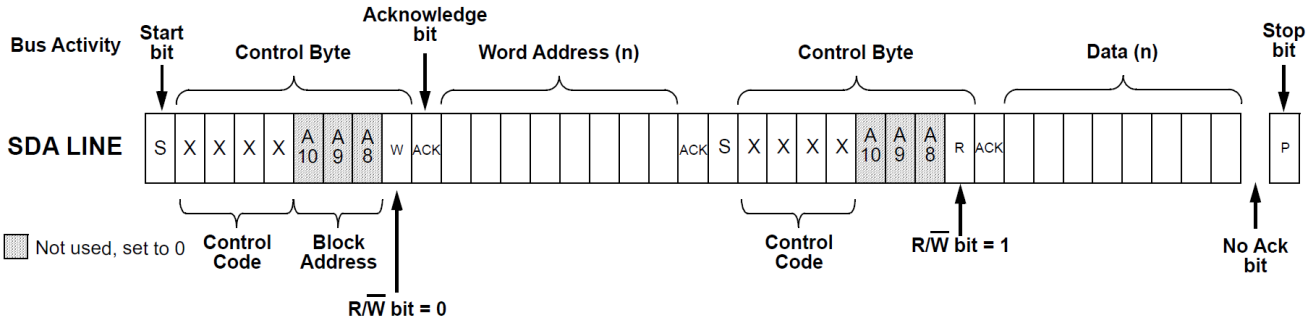


Figure 16：Random Read Command

8.1.3 Sequential Read Command

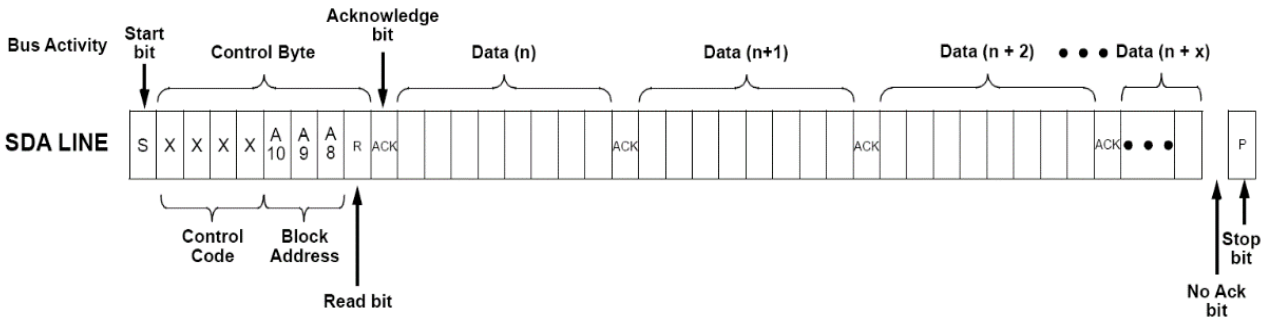


Figure 17：Sequential Read Command

8.2 I²C Write

8.2.1 Byte Write Command

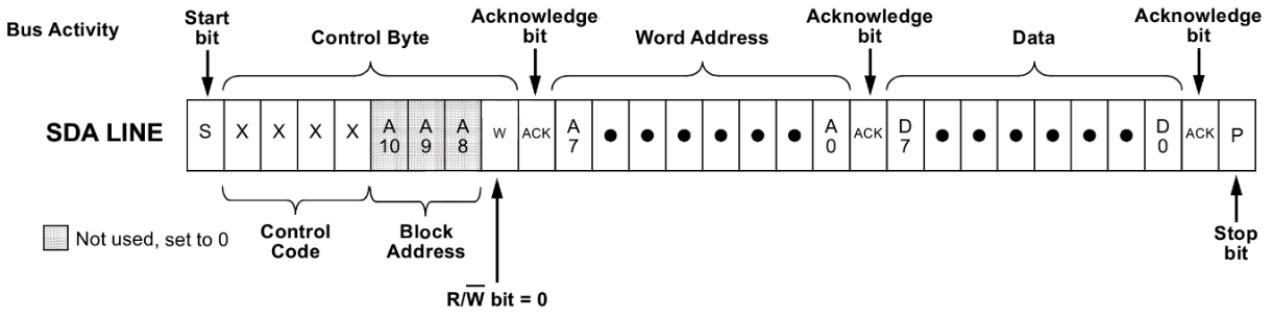


Figure 18：Byte Write Command

8.2.2 Sequential Write Command

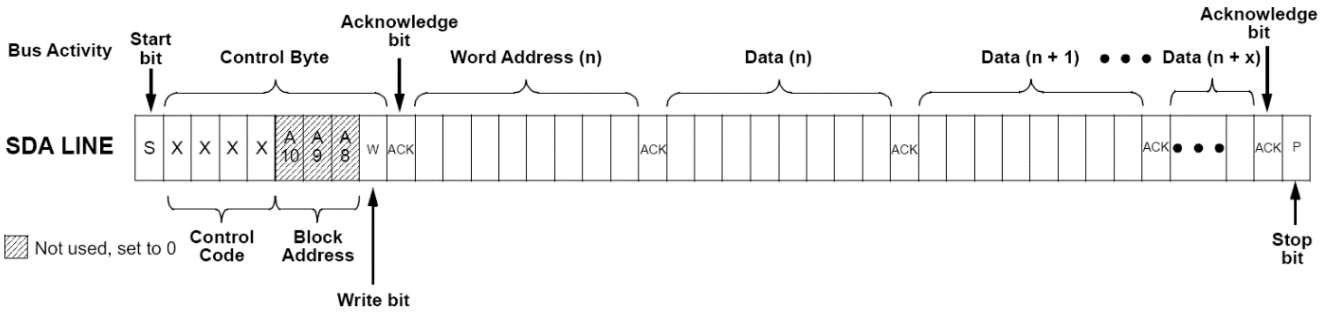


Figure 19：Sequential Write Command

8.3 I²C Timing Diagram

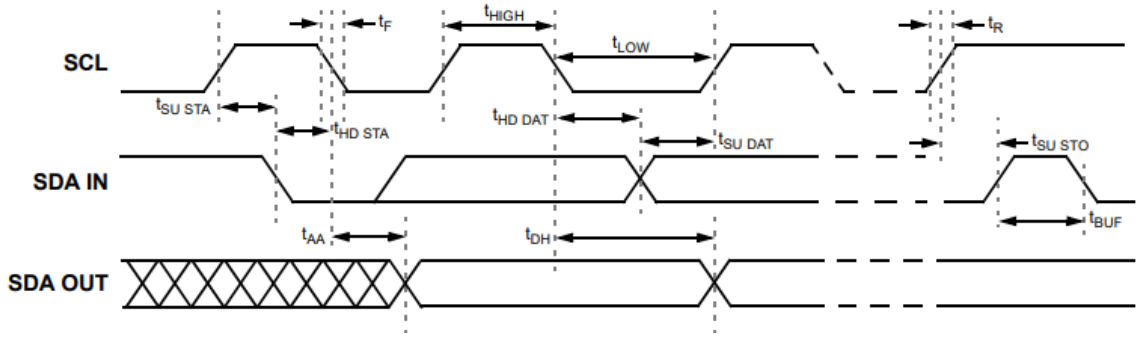


Figure 20：I²C Timing Diagram

8.4 I²C Software Reset Function

If the I²C serial communication is established, the device can be reset to its initial power-on conditions, including the configuration of all Macrocells and all connections provided by the connection matrix. It is achieved by setting register [1861] and resetting I²C to "1", which causes the device to enable again the POR sequence, including reloading all register data from NVM. During the POR sequence, the output of the device will be in tristate, and after the reset is completed, the value of the content register [1861] will be automatically set to "0".

9. Voltage Reference (Vref)

9.1 Voltage Reference Overview

Voltage source output block, voltage reference from 8-bit DAC, and then connected to a drive amplifier, amplification factor of 1X, 2X.

9.2 Voltage Reference Source Formula

Vref Output =1.23V/256*D*Gain （D:8 bit DAC's Data Gain:×1 ×2）

PIN3 source current >=2mA

9.3 Voltage Reference Block Diagram

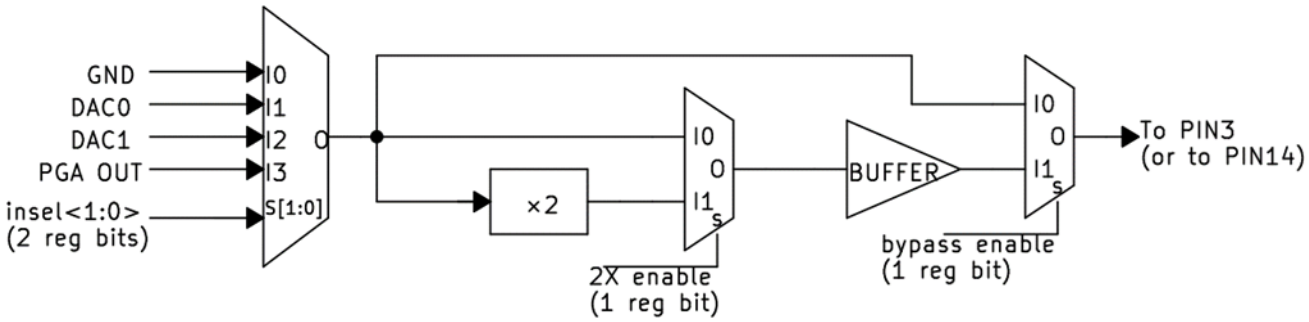


Figure 21：Voltage Reference Block Diagram

10. Digital Comparator (DCMP)

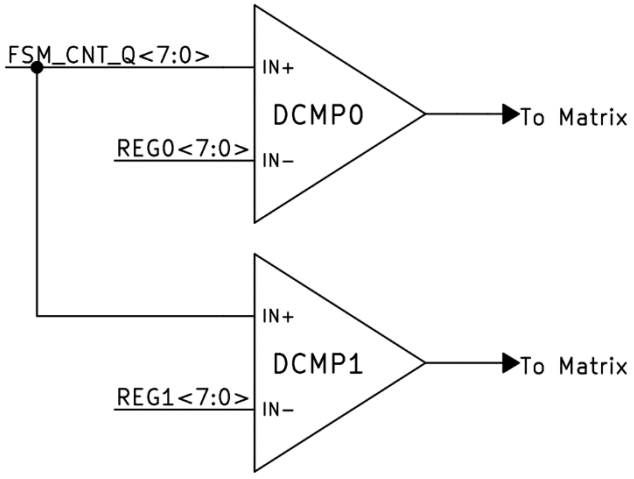


Figure 22：DCMP

11. Analog Comparator (ACMP)

The input of ACMP has 8 channels, and after 8 channels are enabled, the 4 output channels can select any 8 input terminals.

11.1 High Speed ACMP

- Internal VREF: 8bit DAC (=1.23V*‘DAC data’/256)

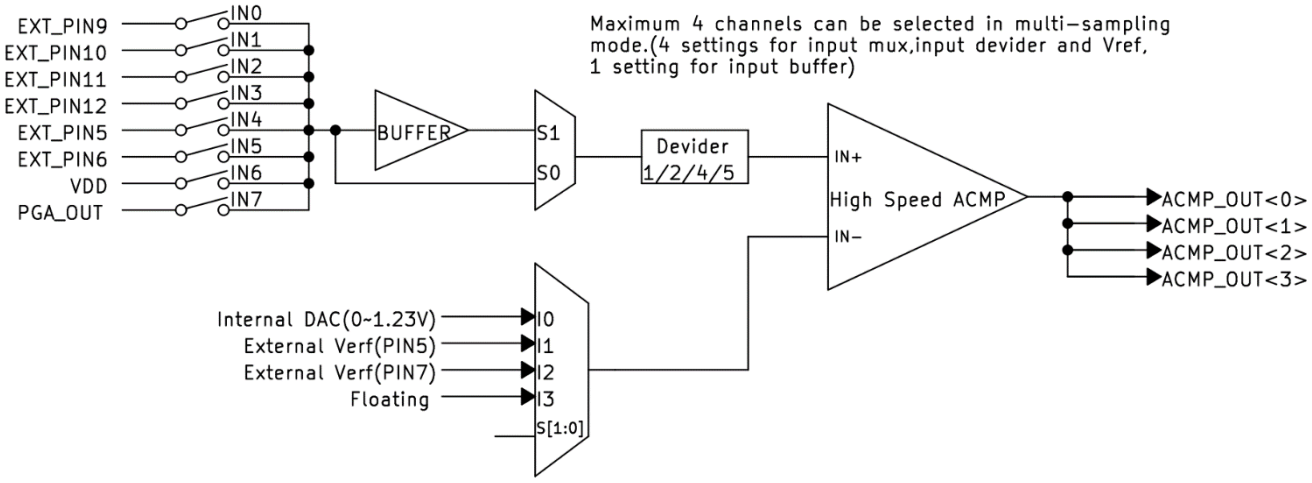


Figure 23：High Speed ACMP

11.2 Low Speed ACMP

- Internal VREF: 8bit DAC (=1.23V*‘DAC data’/256)

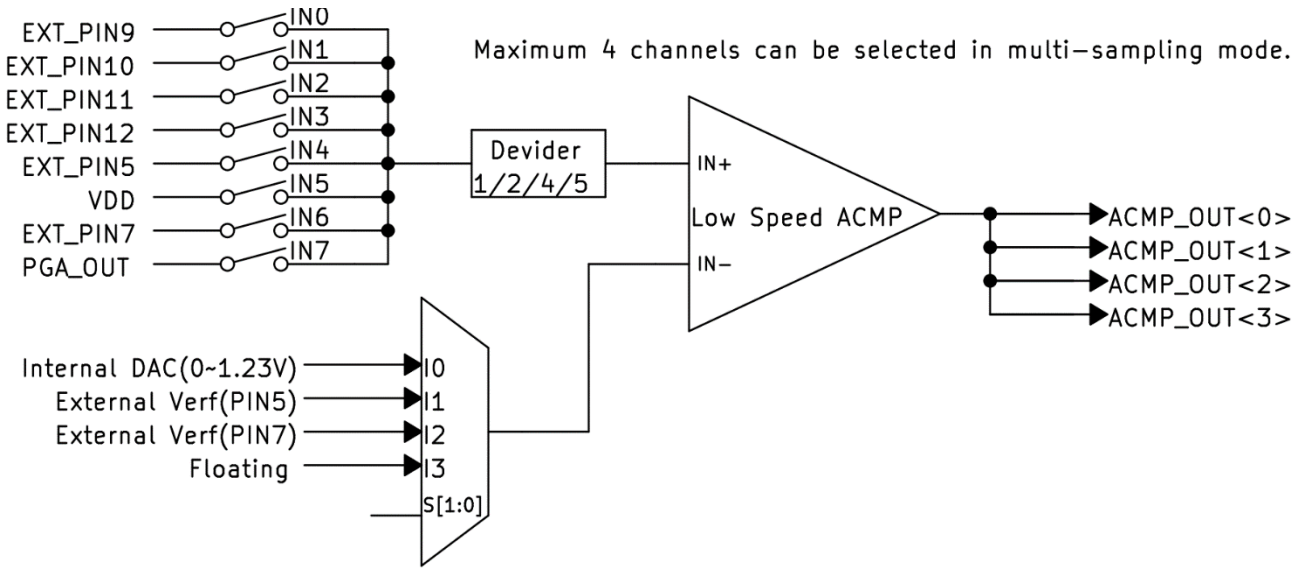


Figure 24：Low Speed ACMP

12. PGA

- Gain: X1, X2, X4, X8 or X16
- Differential Mode
  Vout =$\left[\left(v_{in_+}\right)-\left(v_{in-}\right)\right]*\text{Gain}+V_{CM\_OUT}$
  Input range: $200\text{mV}\le \text{Vcmi}+\left[\left(v_{in_+}\right)-\left(v_{in-}\right)\right]*\text{Gain}\le \text{Vdd}-200\text{mV}$
  Vcmi: Input Common Mode

- Pseudo-Differential Mode
  Vout = $[\left(v_{in_+}\right)-(\text{Voffin\_DAC})]*\text{Gain}+V_{CM\_OUT}$
  Input range: $200\text{mV}\le[\left(v_{in_+}\right)-(\text{Voffin\_DAC})]*\text{Gain}\le \text{Vdd}-200\text{mV}$

- Single Ended Mode
  Vout = Vin * Gain
  Input range: $200\text{mV}\le \text{Vin}*\text{Gain}\le \text{Vdd}-200\text{mV}$

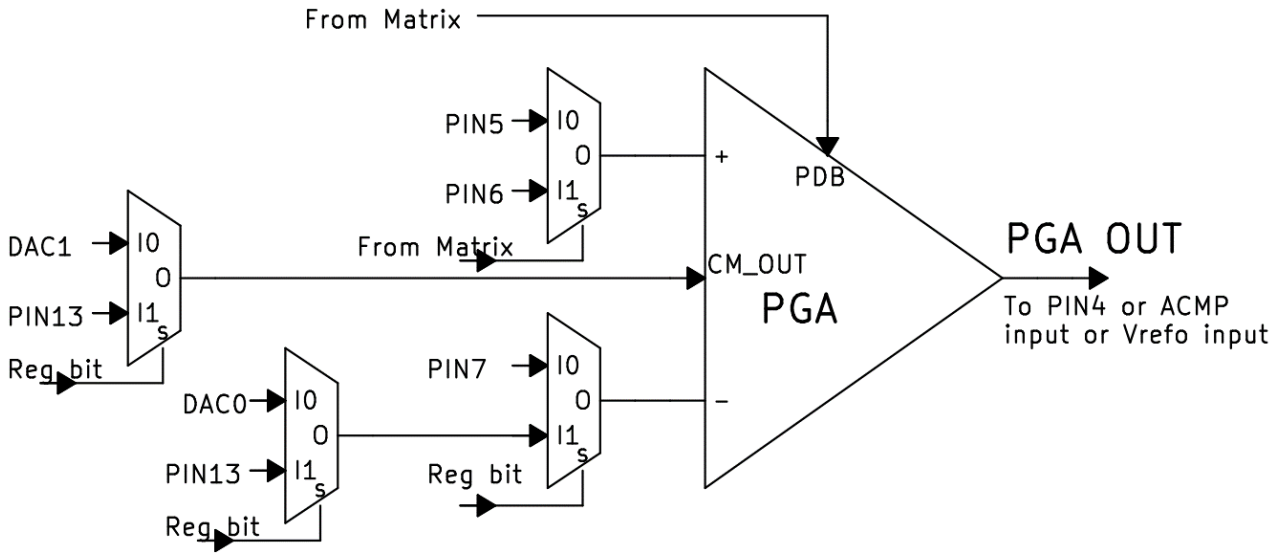


Figure 25：PGA

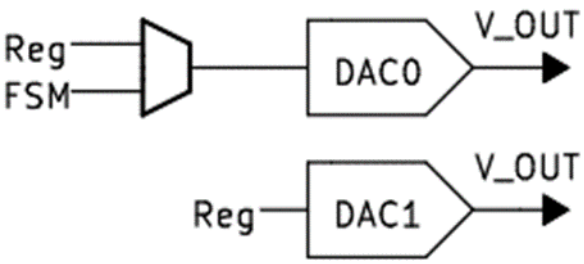


Figure 26：DAC

13. Clock Schem

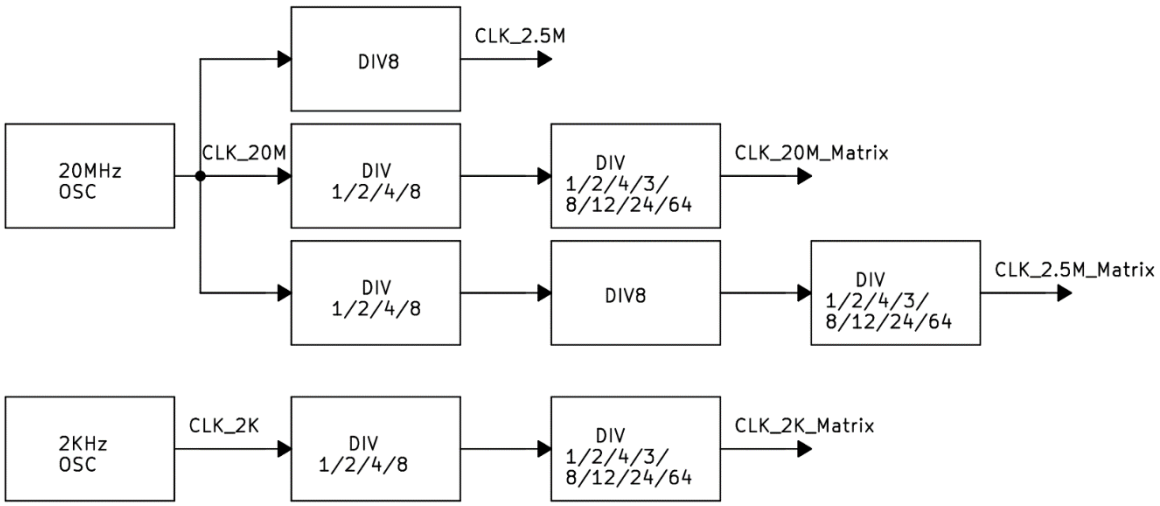


Figure 27：Clock Source

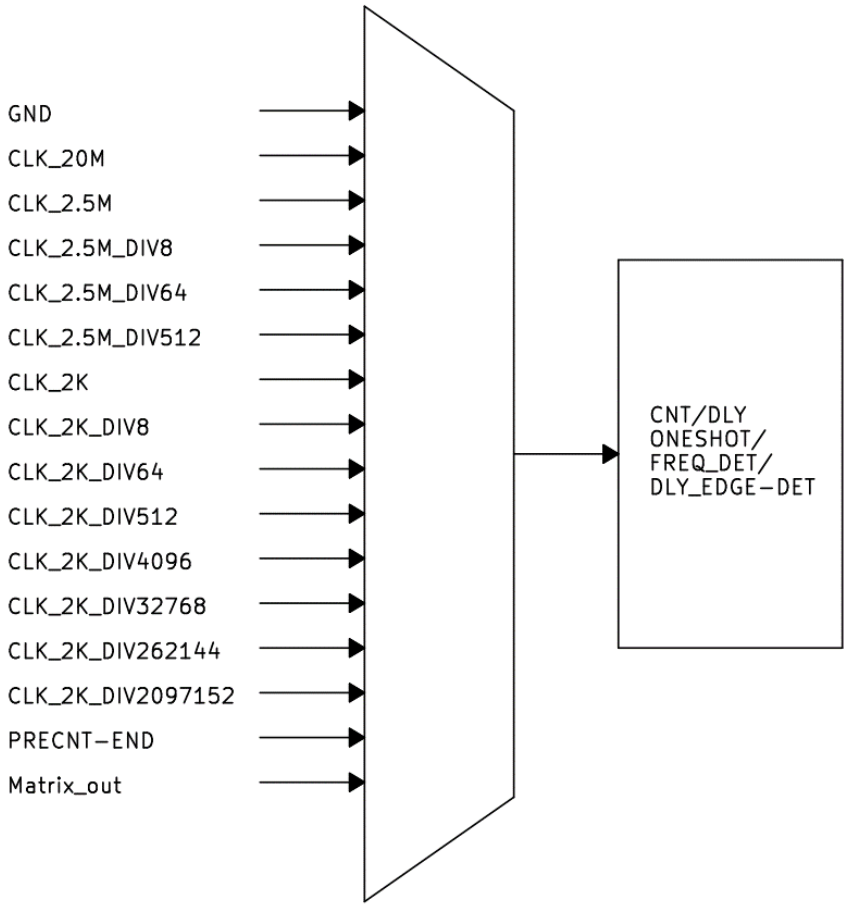


Figure 28：Clock allocation diagram

14. External Clock

LS98102 supports multiple ways to use external high-precision clocks as internal operation reference sources.

14.1 Matrix Source for 2KHz / 2.5MHz / 20MHz Clock

The 20MHz Clock comes from PIN13;
The 2.5MHz clock comes from PIN5;
The 2KHz clock comes from PIN2.

15. Code Protection Function

LS98102 provides the customer with a code protection function, when the protection bit [1863] is program into "1", then all chip function related code can be locked, can not be read out, effectively protect the customer's design information.

16. POR

16.1 Power Down

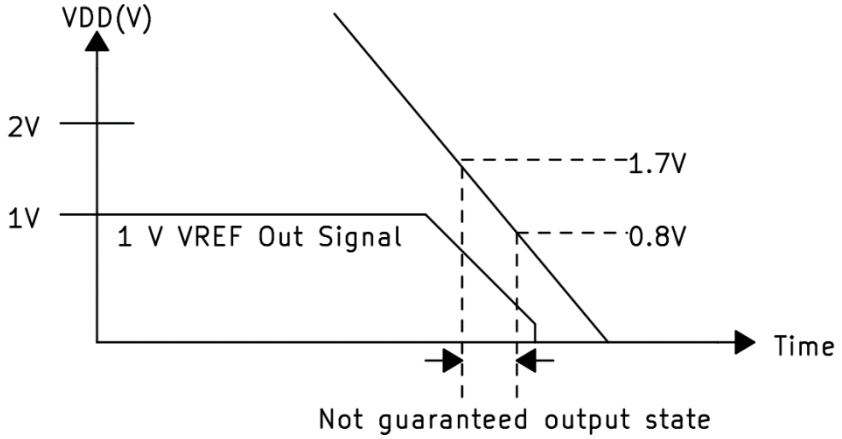


Figure 29：Power Down

During the power down process, when the VDD drops below the Power off Threshold, all macrocells in the LS98102 will be close down. Please take notice that during the slow frequency down period, the output may switch states during this period.

16.2 POR Sequence

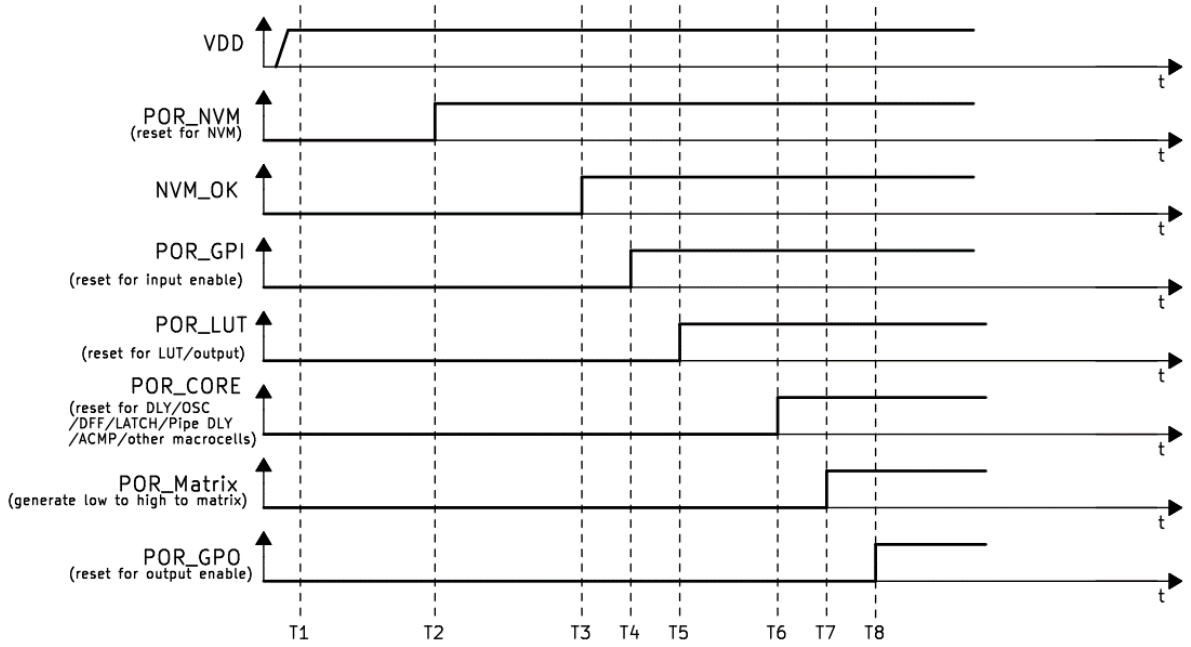


Figure 30：POR Sequence

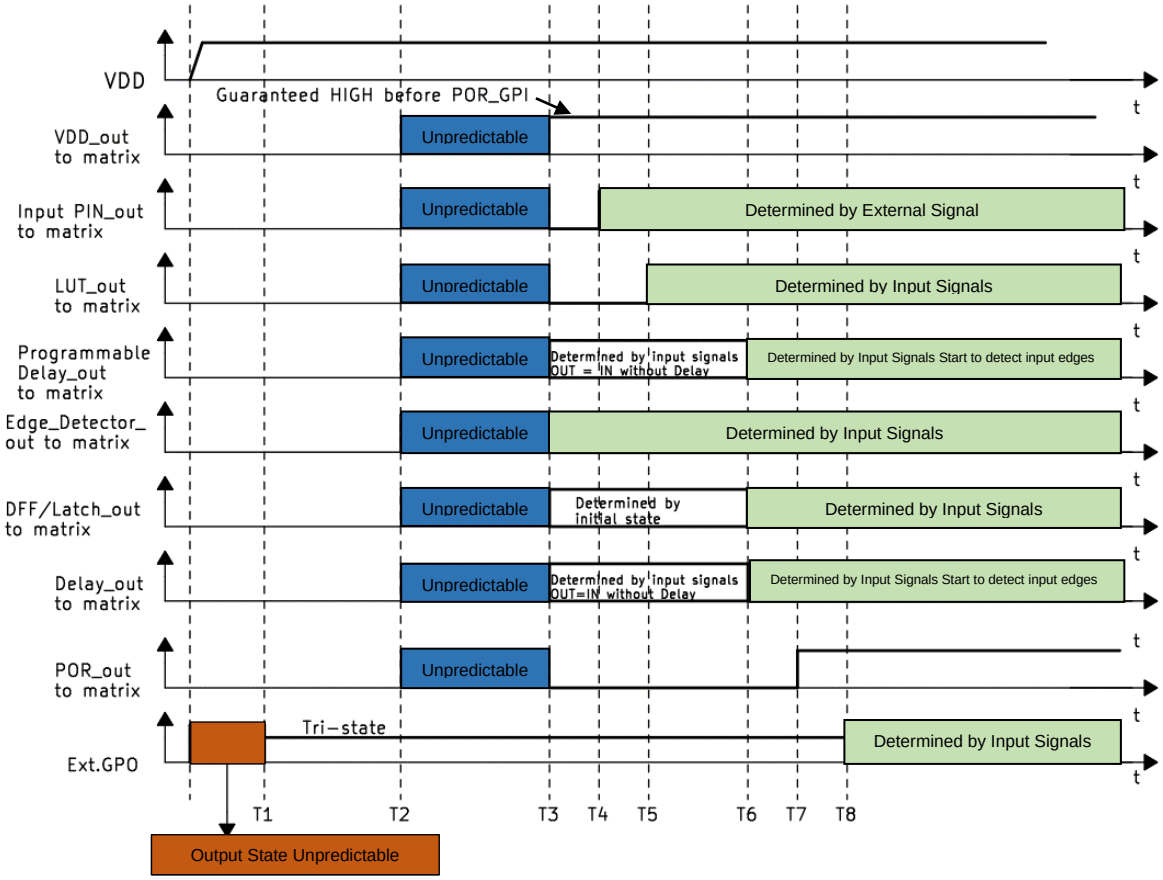


Figure 31：Internal Macrocell States during POR sequence

Note: T1-T8 in Figure 30 and Figure 31 correspond one-to-one.

17. Virtual Memory

17.1 Virtual Memory Input

I²C can write register bit [991:984] into the input of the main matrix <23:16>.

17.2 Virtual Memory Output

I²C can read the output of internal nodes through register [999:992], and the following is the relevant configuration information：

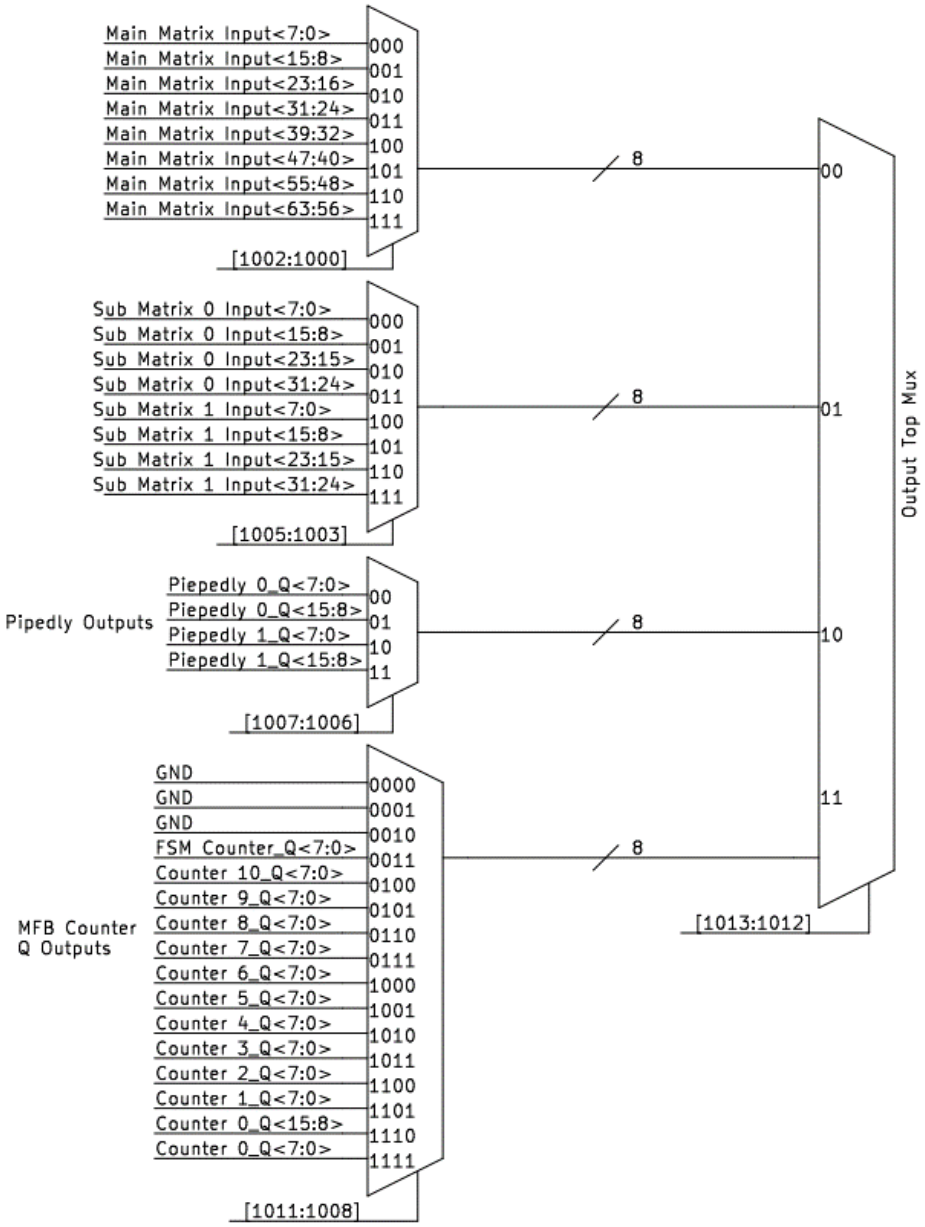
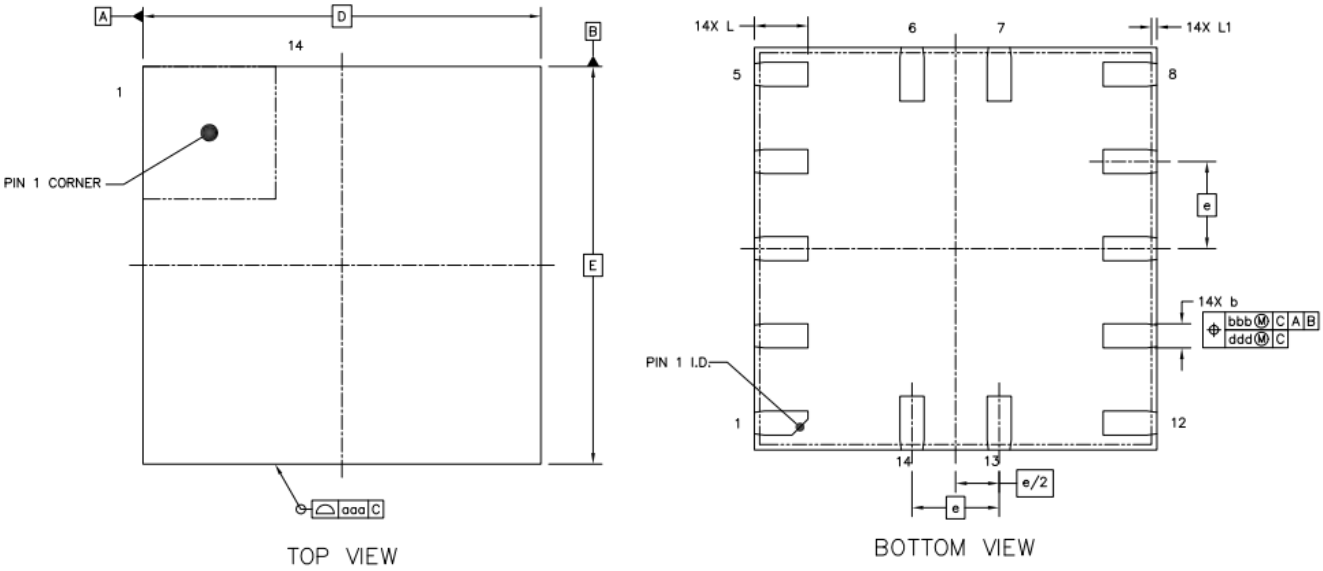
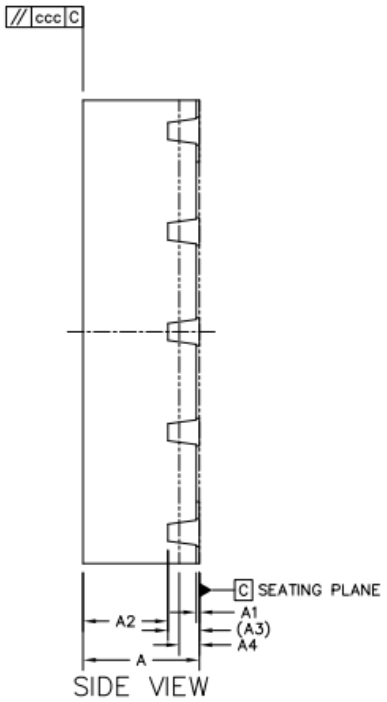


Figure 32：Virtual Memory Out

18. Package Information





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.65 BSC	
LEAD LENGTH		L	0.3	0.4	0.5
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	

Figure 33：Package Outline Diagram

19. Ordering Information

19.1 Tape and Reel Specifications

Table 9：Package Type

Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
QFN-14L 3×3mm	14	3×3×0.75	3000	3000	178/59.8	50	400	50	400	12	8

19.2 Carrier Tape Drawing and Dimensions

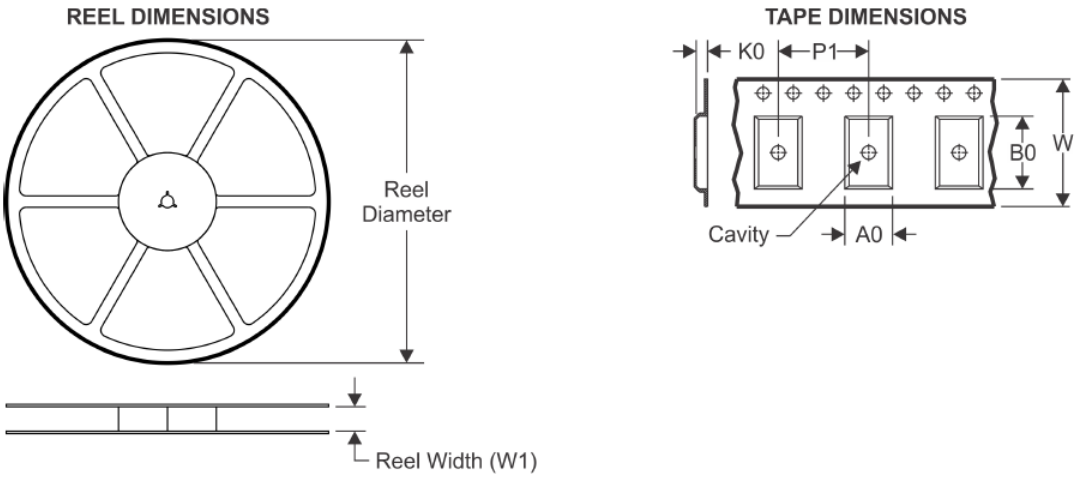


Figure 34：Carrier Tape Drawing and Dimensions

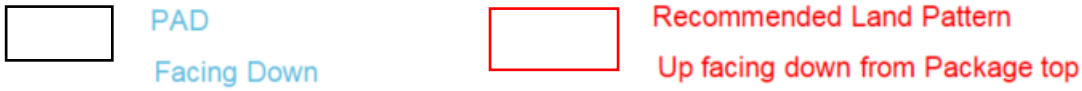
Table 10：Carrier Tape Drawing and Dimensions

A0	Dimension designed to accommodate the component width	3.35mm
B0	Dimension designed to accommodate the component length	3.35mm
K0	Dimension designed to accommodate the component thickness	1.13mm
W	Overall width of the carrier tape	12.00mm
W1	Reel Width	12.80mm
P0	Pitch between Index Hole Pitch	4.00mm
P1	Pitch between successive cavity centers	8.00mm

20. Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020

20.1 Recommended Land Pattern



3.0mm x 3.0mm

QFN-14

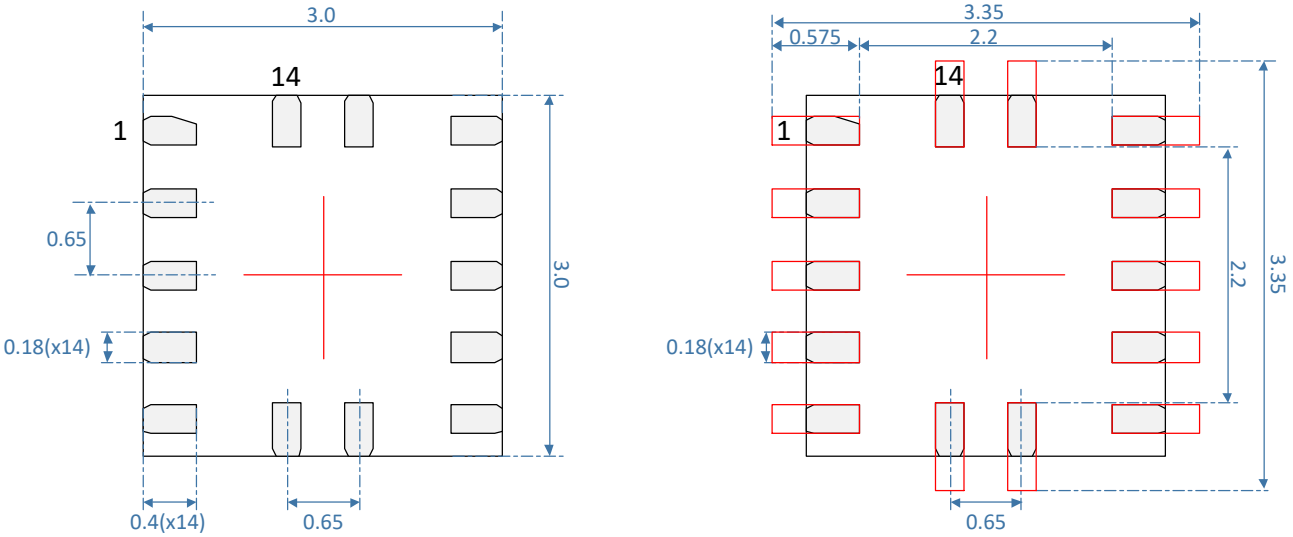


Figure 35：Recommended Land Pattern

21. Revision History

Table 11：Revision History

Version	Revision Contents	Revised By	Date
R01	Initial version		2023-10-25
R02	1.Change 'To PIN4 or to PIN14' in Figure 21 to 'To PIN3 or to PIN14'(P29) 2. Add 'Input Range Formula' toPGA (P31)		2023-12-06
R03	1.Update the Gain parameter values of ACMPH/ACMPL Specifications in Tables 5 to 7 and the voltage range of V_{ACMP} parameter 'Negative Input' should be changed from 0~1V to 0~1.23V (p11, p14, P17) 2. Adjust the IO PIN module in Table 7 according to the test addition data, and update the Max value of V_{IL} parameter 0.71 under 'Low-Level Logic Input' condition to 0.85 (P15). 3. Remove Section 9.1 "Track-to-track Description of output capability" (P29)		2024-01-08