Product Introduction

LS98006 is a general and configurable analog digital hybrid chip, characterized by small size, ultra-low power consumption, and high reliability. Customers can design chips based on their own functional requirements, configure the connections between the simulation and logic functional macrocell inside LS98006, and burn the design into the internal NVM (Non-Volatile Memory). The internal functional blocks are as follows:

- Three Analog Comparators
  - One Multi-Channel Analog Comparator (MACMP)
  - One Single-Channel Analog Comparator (ACMP1)
  - One Single-Channel Analog Comparator (ACMP2)
- Two Voltage Reference Outputs
- Thirty-nine Combination Function Macrocells
  - Seven 2-bit LUT/DFF
  - Three 2-bit LUT/Pattern Generator
  - Six 2-bit LUT/Edge Detector
  - Twenty 3-bit LUT/DFF
  - Three 3-bit LUT/36-bit Pipe Delay
- Sixteen Multi-Function Blocks (MFB)
  - Twelve Selectable 3-bit LUT/DFF + 8-bit Counter/Delay
  - Four Selectable 4-bit LUT/DFF + 16-bit Counter/Delay
- One I^2C Virtual Output and 12-bits Pipe Delay
- I^2C Protocol Interface
- Three Internal Oscillators
  - One 20MHz Oscillator
  - One 2MHz Oscillator
  - One 2KHz Oscillator
- Crystal Oscillator
- External Clock
- Two Constant-Current Source（Maximum 3mA）
- Power-On Reset (POR)
- The Read Protection Function
- Wide Range Power Supply VDD: 1.8V(±5 %) to 5 V (±10 %)
- Operating Temperature Range: -40℃ to 85℃
- RoHS Compliant/Halogen-Free
- Package: 20pin TQFN: 2mm x 3mm x 0.55mm, 0.4mm pin pitch
  20pin TSSOP: 6.5mm×6.4mm×1.0mm, 0.65mm pin pitch

Applications

- Personal Computers and Servers
- The Internet of things device
- PC Peripherals
- Handheld and Portable Electronics
- Consumer Electronics
- Data Communications Equipment
- Industrial Control and Instrument
- Vehicle Central Control and Instrument
- Security Equipment
- Medical Equipment
- Motor Control
- Energy Storage Equipment

Glossary

A

- ACMP: Analog Comparator
- ACMPH: Analog Comparator High Speed
- ACMPL: Analog Comparator Low Speed

B

- BG: Bandgap

C

- CLK: Clock
- CNT: Counter

D

- DFF: D Flip-Flop
- DLY: Delay

E

- ESD: Electrostatic discharge

F

- FSM: Finite State Machine

G

- GPI: General Purpose Input
- GPIO: General Purpose Input/Output
- GPO: General Purpose Output

I

- IN: Input
- IO: Input/Output

L

- LSB: Least Significant Bit
- LUT: Look-Up Table
- LV: Low Voltage

M

- MSB: Most Significant Bit
- MUX: Multiplexer
- MFB: Multi-Function Block
- MSL: Moisture Sensitivity Level

N

- nRST: Reset
- NVM: Non-Volatile Memory

O

- OE: Output Enable
- OSC: Oscillator
- OUT: Output

P

- PDWM: Power-down
- PGen: Pattern Generator
- POR: Power-On Reset
- PP: Push-Pull
- PDLY: Programmable Delay

S

- SCL: I^2C Clock Input
- SDA: I^2C Data Input/Output
- SLA: Slave Address
- SMT: With Schmitt Trigger

V

- VREF: Voltage Reference

W

- WOSMT: Without Schmitt Trigger

Contents

1. System Block

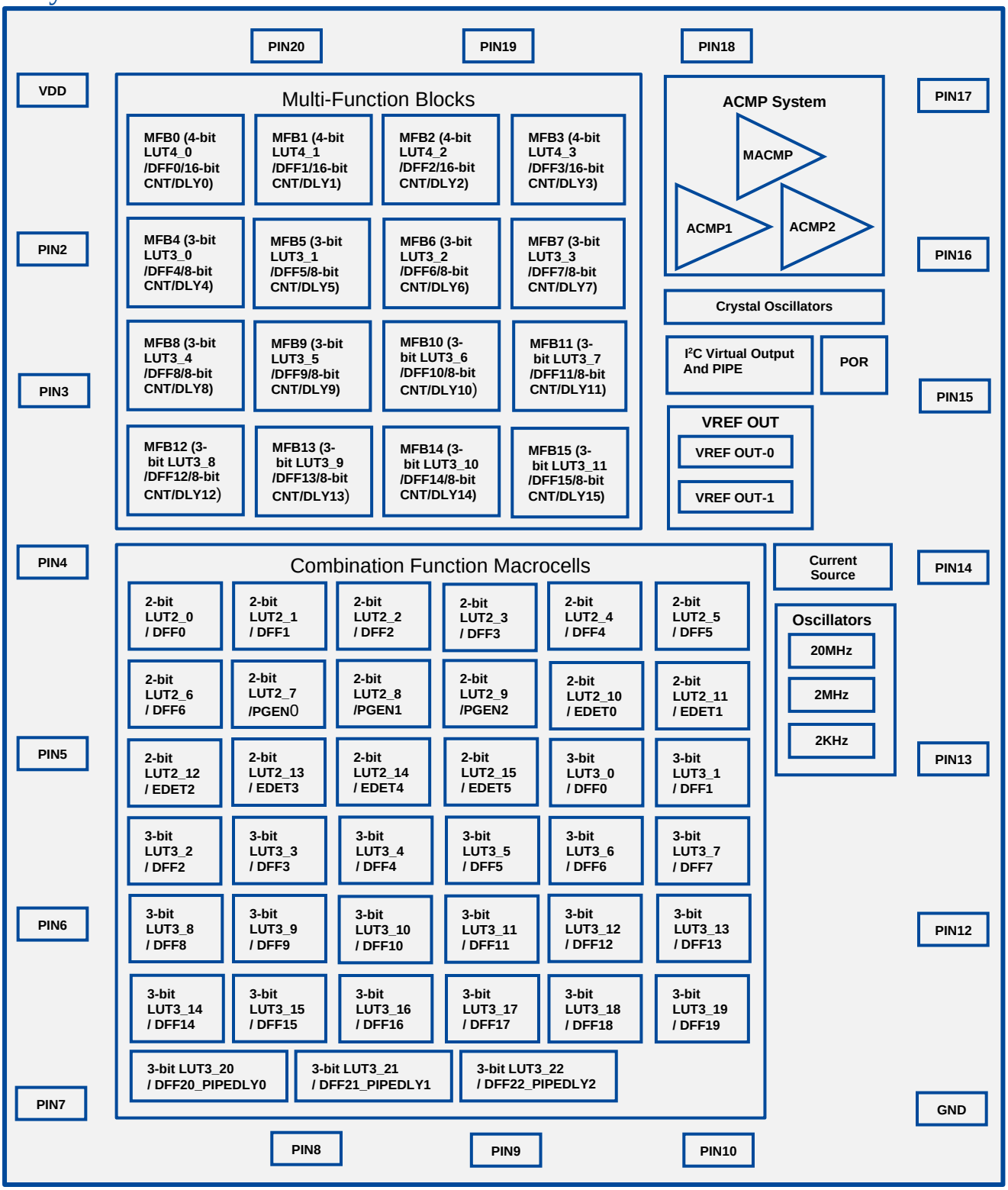


Figure 1: Block Diagram

2. Pin Definition

2.1 Pin Configuration-TQFN-20L

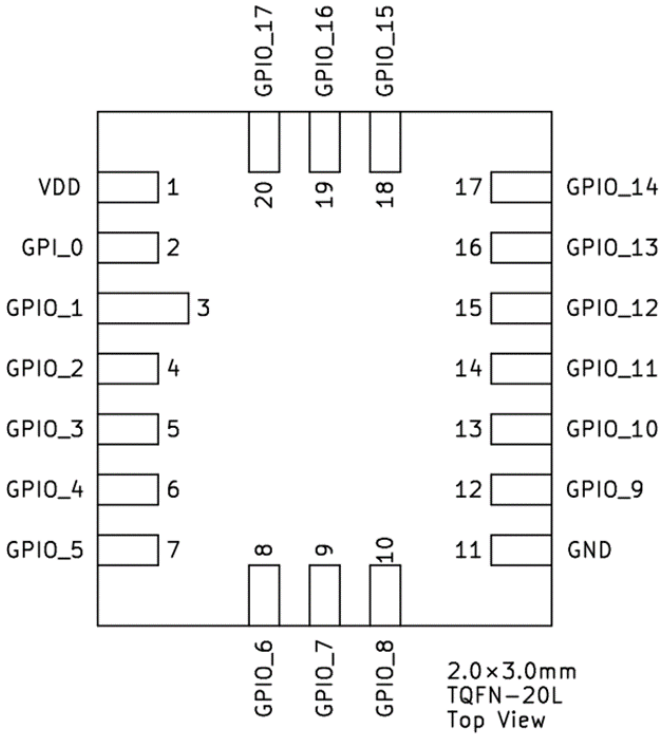


Figure 2：TQFN-20L (TOP View)

2.2 Pin Function Description

Table 1：Pin Function Description

Pin	Name	Type	Function
1	VDD	Power Source	Positive Power Input
2	GPI_0	GPI	Digital Input
		SLA_0	I²C Slave address bit 0
		VPP	OTP Program Power
3	GPIO_1	GPIO1, SLA-1	Digital Input/Output, I²C Slave address bit 1
4	GPIO_2	GPIO2, SLA-2	Digital Input/Output, I²C Slave address bit 2
5	GPIO_3	GPIO3, SLA-3	Digital Input/Output, I²C Slave address bit 3
		Analog IO	Analog Input
6	GPIO_4	GPIO4	Digital Input/Output
		Analog IO	Analog Input
7	GPIO_5	GPIO5	Digital Input/Output
		Analog IO	Analog Input
8	GPIO_6	GPIO6	Digital Input/Output
		I²C-SCL	I²C Clock
9	GPIO_7	GPIO7	Digital Input/Output
		I²C-SDA	I²C Data
10	GPIO_8	GPIO8	Digital Input/Output
		Analog IO	Analog Input
11	GND	GND	Power Grounding
12	GPIO_9	GPIO9	Digital Input/Output
		Analog IO	Analog Input
13	GPIO_10	GPIO10	Digital Input/Output
		Analog IO	Analog Input
14	GPIO_11	GPIO11	Digital Input/Output
		Analog IO	Analog Input
15	GPIO_12	GPIO12	Digital Input/Output
		Analog IO	Analog Input
16	GPIO_13	GPIO13	Digital Input/Output
		XTAL-0	External Crystal Output
17	GPIO_14	GPIO14	Digital Input/Output
		XTAL-1	External Crystal Input
18	GPIO_15	GPIO15	Digital Input/Output
		VREF0	VREF 0 Output
19	GPIO_16	GPIO16	Digital Input/Output
		VREF1	VREF 1 Output
20	GPIO_17	GPIO17	Digital Input/Output

3. Characteristics

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Analog and digital grounds must be connected together on the PCB board. The place of connection depends on customers' schematic. For application cases with low digital current of LS98006, both AGND and GND should be connected to analog ground plane.

Table 2: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VDD to GND	-0.3	7	V
IO maximum voltage	-0.3	7	V
VDD to GND Maximum DC current	--	180	mA
Input leakage current	--	1000	nA
Storage temperature	-65	150	℃
Junction temperature	--	150	℃
Moisture Sensitivity Level (MSL)	1		

3.2 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Min	Max	Unit
VDD Supply Voltage	1.71	5.5	V
Operating Temperature	-40	85	℃
Maximum voltage input to Pin	-0.2	VDD +0.3	V
Capacitor Value at VDD	0.1	--	uF

3.3 Electrostatic Discharge Ratings

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Charged Device Model)	500	--	V
ESD Protection (Human Body Model)	2000	--	V

3.4 Electrical Characteristics

Table 5：Electrical Characteristics (VDD: 1.8 V ±5%, Temp: -40~85°C)

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
POR						
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.3	1.43	1.6	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.55	1.03	1.35	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	0.8	--	ms
I_{stand_by}		T=+25 °C	--	50	--	nA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7*VDD	--	--	V
		Logic Input with Schmitt Trigger	0.8*VDD	--	--	V
		Low-Level Logic Input	0.83	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.3*VDD	V
		Logic Input with Schmitt Trigger	--	--	0.2*VDD	V
		Low-Level Logic Input	--	--	0.46	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.42	--	V
I_{LKG}	Input leakage (Absolute Value)	--	--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 100 µA, 1X Drive	1.69	--	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive	1.70	--	--	V
		Push-Pull, I_{OH} = 100 µA, 4X Drive	1.71	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 100 µA, 1X Drive	--	--	0.012	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive	--	--	0.006	V
		Push-Pull, I_{OL} = 100 µA, 4X Drive	--	--	0.003	V
		Open Drain, I_{OL} = 100 µA, 1X Drive	--	--	0.004	V
		Open Drain, I_{OL} = 100 µA, 2X Drive	--	--	0.002	V
		Open Drain, I_{OL} = 100 µA, 4X Drive	--	--	0.001	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push-Pull, V_{OH} = VDD-0.2, 1X Drive	0.81	--	--	mA
		Push-Pull, V_{OH} = VDD-0.2, 2X Drive	1.6	--	--	mA
		Push-Pull, V_{OH} = VDD-0.2, 4X Drive	3.2	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push-Pull, V_{OL} = 0.15 V, 1X Drive	1.1	--	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive	2.1	--	--	mA
		Push-Pull, V_{OL} = 0.15 V, 4X Drive	4.2	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Drive	3.2	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Drive	6.3	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 4X Drive	12.7	--	--	mA
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	KΩ
		10 k Pull Up	--	10	--	KΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	KΩ
		10 k Pull Down	--	10	--	KΩ
Oscillators						
Power-On time	20MHz OSC	T=+25 °C	--	2.4	--	uS
$Frequency_{Accuracy}$		T=+25 °C	--	20	--	MHz
		T=-40 °C to +85 °C	19	--	21	MHz

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
Power Consumption		T=+25 °C	--	73	--	uA
Power-On time	2MHz OSC	T=+25 °C	--	0.5	--	uS
$Frequency_{Accuracy}$		T=+25 °C	--	2	--	MHz
		T=-40 °C to +85 °C	1.84	--	2.16	MHz
Power Consumption		T=+25 °C	--	28	--	uA
Power-On time	2KHz OSC	T=+25 °C	--	520	--	uS
$Frequency_{Accuracy}$		T=+25 °C	--	2	--	KHz
		T=-40 °C to +85 °C	1.9	--	2.1	KHz
Power Consumption		T=+25 °C	--	0.22	--	uA
ACMP Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1	V
V_{offset}	ACMP Input Offset	--	-3	1	3	mV
$MACMP_{Voffset}$	Channel switching frequency	Freq=75K/37.5K	-4	--	4	mV
		Freq=150K	-10	--	10	mV
Input Buffer (VDD>2.3V)	Bandwidth	Input Buffer	--	1	--	MHz
	Offset		-10	2.5	10	mV
	Power Consumption		--	6	--	uA
t_{start}	ACMP Startup Time when BG On	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMP	--	45	65	uS
	ACMP Startup Time when BG Off		--	175	245	uS
R_{sin}	Series Input Resistance	Gain = 1	--	100	--	MΩ
		Gain = 1/2	1.52	1.9	2.28	MΩ
		Gain = 1/4	1.52	1.9	2.28	MΩ
		Gain = 1/6	1.52	1.9	2.28	MΩ
PROP	Propagation Delay, Response Time	ACMPxL, Vref =1V, Gain = 1, Overdrive = 20 mV	--	1.1	--	uS
G	Gain error	G=1	--	--	--	
		G=1/2	-0.5%	--	0.5%	
		G=1/4	-0.5%	--	0.5%	
		G=1/6	-0.5%	--	0.5%	
Vref	Internal Vref error, Vref=0 to1000 mV	T=+25 °C	-0.5%	--	0.5%	Fs
		T=-40 °C to +85 °C	-1%	--	1%	Fs
Power Consumption			--	12	--	uA
Vref Out Characteristics						
$Vref_{Accuracy}$	Vref Gain Accuracy	G=1	-0.2%	--	0.2%	
		G=2	-0.2%	--	0.2%	
		G=4	-0.2%	--	0.2%	
		G=5	-0.2%	--	0.2%	
$Vref_{offset}$	Vref Opamp Offset	G=1 (VCM IN=VDD/2)	-3.5	--	3.5	mV
Vref DAC_{offset}			--	7.5	--	mV
$I_{loading}$		Push Pull Output	2	--	--	mA
Power Consumption			--	10	--	uA
Voltage of Output to VDD		Maximum output voltage $\mathrm{Vout} = \mathrm{VDD} - 0.3 - 300\Omega \times \mathrm{Iout}$				
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

Table 6：Electrical Characteristics (VDD: 3.3 V ±10%, Temp: -40~85°C)

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
POR						
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.3	1.43	1.6	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.55	1.03	1.35	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	0.4	0.8	1.3	ms
I_{stand_by}		T=+25 °C	--	80	--	nA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7*VDD	--	--	V
		Logic Input with Schmitt Trigger	0.8*VDD	--	--	V
		Low-Level Logic Input	1.02	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.3*VDD	V
		Logic Input with Schmitt Trigger	--	--	0.2*VDD	V
		Low-Level Logic Input	--	--	0.63	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.45	--	V
I_{LKG}	Input leakage (Absolute Value)	--	--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 3 mA, 1X Drive	2.67	--	--	V
		Push-Pull, I_{OH} = 3 mA , 2X Drive	2.85	--	--	V
		Push-Pull, I_{OH} = 3 mA , 4X Drive	2.93	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 3 mA , 1X Drive	--	--	0.21	V
		Push-Pull, I_{OL} = 3 mA , 2X Drive	--	--	0.10	V
		Push-Pull, I_{OL} = 3 mA , 4X Drive	--	--	0.05	V
		Open Drain, I_{OL} = 3 mA , 1X Drive	--	--	0.07	V
		Open Drain, I_{OL} = 3 mA , 2X Drive	--	--	0.03	V
		Open Drain, I_{OL} = 3 mA , 4X Drive	--	--	0.02	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push-Pull, V_{OH} = 2.4 V, 1X Drive	5	--	--	mA
		Push-Pull, V_{OH} = 2.4 V , 2X Drive	10	--	--	mA
		Push-Pull, V_{OH} = 2.4 V , 4X Drive	20	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push-Pull, V_{OL} = 0.4 V, 1X Drive	5	--	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	10	--	--	mA
		Push-Pull, V_{OL} = 0.4 V, 4X Drive	19.9	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	15.2	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	30.3	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 4X Drive	54	--	--	mA
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	KΩ
		10 k Pull Up	--	10	--	KΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	KΩ
		10 k Pull Down	--	10	--	KΩ
Oscillators						
Power-On time	20MHz OSC	T=+25 °C	--	2.2	--	uS
$Frequency_{Accuracy}$		T=+25 °C	--	20	--	MHz
		T=-40 °C to +85 °C	19	--	21	MHz
Power Consumption		T=+25 °C	--	73	--	uA

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
Power-On time	2MHz OSC	T=+25 °C	--	0.5	--	uS
$Frequency_{Accuracy}$		T=+25 °C	--	2	--	MHz
		T=-40 °C to +85 °C	1.84		2.16	MHz
Power Consumption		T=+25 °C	--	28	--	uA
Power-On time	2KHz OSC	T=+25 °C	--	520	--	uS
$Frequency_{Accuracy}$		T=+25 °C	--	2	--	KHz
		T=-40 °C to +85 °C	1.9	--	2.1	KHz
Power Consumption		T=+25 °C	--	0.22	--	uA
ACMP Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1	V
V_{offset}	ACMP Input Offset	--	-3	1	3	mV
$MACMP_{Voffset}$	Channel switching frequency	Freq=75K/37.5K	-4	--	4	mV
		Freq=150K	-10	--	10	mV
Input Buffer (VDD>2.3V)	Bandwidth	Input Buffer	--	1	--	MHz
	Offset		-10	2.5	10	mV
	Power Consumption		--	6	--	uA
t_{start}	ACMP Startup Time when BG On	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMP	--	45	65	uS
	ACMP Startup Time when BG Off		--	175	245	uS
R_{sin}	Series Input Resistance	Gain = 1	--	100	--	MΩ
		Gain = 1/2	1.52	1.9	2.28	MΩ
		Gain = 1/4	1.52	1.9	2.28	MΩ
		Gain = 1/6	1.52	1.9	2.28	MΩ
PROP	Propagation Delay, Response Time	ACMPxL, Vref =1V, Gain = 1, Overdrive = 20 mV	--	1.1	--	uS
G	Gain error	G=1	--	--	--	
		G=1/2	-0.5%	--	0.5%	
		G=1/4	-0.5%	--	0.5%	
		G=1/6	-0.5%	--	0.5%	
Vref	Internal Vref error, Vref=0 to1000 mV	T=+25 °C	-0.5%	--	0.5%	Fs
		T=-40 °C to +85 °C	-1%	--	1%	Fs
Power Consumption			--	12	--	uA
Vref Out Characteristics						
$Vref_{Accuracy}$	Vref Gain Accuracy	G=1	-0.2%	--	0.2%	
		G=2	-0.2%	--	0.2%	
		G=4	-0.2%	--	0.2%	
		G=5	-0.2%	--	0.2%	
$Vref_{offset}$	Vref Opamp Offset	G=1 (VCM IN=VDD/2)	-3.5	--	3.5	mV
Vref DAC_{offset}			--	7.5	--	mV
$I_{loading}$		Push Pull Output	2	--	--	mA
Power Consumption			--	10	--	uA
Voltage of Output to VDD		Maximum output voltage $\mathrm{Vout} = \mathrm{VDD} - 0.3 - 300\Omega \times \mathrm{Iout}$				
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

Table 7：Electrical Characteristics (VDD: 5 V ±10%, Temp: -40~85°C)

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
POR						
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.3	1.43	1.6	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.55	1.03	1.35	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	0.4	0.8	1.3	ms
I_{stand_by}		T=+25 °C	--	150	--	nA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7*VDD	--	--	V
		Logic Input with Schmitt Trigger	0.8*VDD	--	--	V
		Low-Level Logic Input	1.11	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.3*VDD	V
		Logic Input with Schmitt Trigger	--	--	0.2*VDD	V
		Low-Level Logic Input	--	--	0.70	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.54	--	V
I_{LKG}	Input leakage (Absolute Value)	--	--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} =5 mA, 1X Drive	4.16	--	--	V
		Push-Pull, I_{OH} = 5 mA , 2X Drive	4.33	--	--	V
		Push-Pull, I_{OH} = 5 mA , 4X Drive	4.41	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 5 mA , 1X Drive	--	--	0.26	V
		Push-Pull, I_{OL} = 5 mA , 2X Drive	--	--	0.12	V
		Push-Pull, I_{OL} = 5 mA , 4X Drive	--	--	0.06	V
		Open Drain, I_{OL} = 5 mA , 1X Drive	--	--	0.08	V
		Open Drain, I_{OL} = 5 mA , 2X Drive	--	--	0.04	V
		Open Drain, I_{OL} = 5 mA , 4X Drive	--	--	0.02	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push-Pull, V_{OH} = 2.4 V, 1X Drive	19.2	--	--	mA
		Push-Pull, V_{OH} = 2.4 V , 2X Drive	38.5	--	--	mA
		Push-Pull, V_{OH} = 2.4 V , 4X Drive	70	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push-Pull, V_{OL} = 0.4 V, 1X Drive	7.1	--	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	14.2	--	--	mA
		Push-Pull, V_{OL} = 0.4 V, 4X Drive	28.4	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	21.7	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	43.4	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 4X Drive	79	--	--	mA
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	KΩ
		10 k Pull Up	--	10	--	KΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	KΩ
		10 k Pull Down	--	10	--	KΩ
Oscillators						
Power-On time	20MHz OSC	T=+25 °C	--	2.2	--	uS
$Frequency_{Accuracy}$		T=+25 °C	--	20	--	MHz
		T=-40 °C to +85 °C	19	--	21	MHz
Power Consumption		T=+25 °C	--	73	--	uA

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
Power-On time	2MHz OSC	T=+25 °C	--	0.5	--	uS
$Frequency_{Accuracy}$		T=+25 °C	--	2	--	MHz
		T=-40 °C to +85 °C	1.84	--	2.16	MHz
Power Consumption		T=+25 °C	--	28	--	uA
Power-On time	2kHz OSC	T=+25 °C	--	520	--	uS
$Frequency_{Accuracy}$		T=+25 °C	--	2	--	KHz
		T=-40 °C to +85 °C	1.9	--	2.1	KHz
Power Consumption		T=+25 °C	--	0.22	--	uA
ACMP Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1	V
V_{offset}	ACMP Input Offset	--	-3	1	3	mV
$MACMP_{Voffset}$	Channel switching frequency	Freq=75K/37.5K	-4	--	4	mV
		Freq=150K	-10	--	10	mV
Input Buffer (VDD>2.3V)	Bandwidth	Input Buffer	--	1	--	MHz
	Offset		-10	2.5	10	mV
	Power Consumption		--	6	--	uA
t_{start}	ACMP Startup Time when BG On	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMP	--	45	65	uS
	ACMP Startup Time when BG Off		--	175	245	uS
R_{sin}	Series Input Resistance	Gain = 1	--	100	--	MΩ
		Gain = 1/2	1.52	1.9	2.28	MΩ
		Gain = 1/4	1.52	1.9	2.28	MΩ
		Gain = 1/6	1.52	1.9	2.28	MΩ
PROP	Propagation Delay, Response Time	ACMPxL, Vref =1V, Gain = 1, Overdrive = 20 mV	--	1.1	--	uS
G	Gain error	G=1	--	--	--	
		G=1/2	-0.5%	--	0.5%	
		G=1/4	-0.5%	--	0.5%	
		G=1/6	-0.5%	--	0.5%	
Vref	Internal Vref error, Vref=0 to1000 mV	T=+25 °C	-0.5%	--	0.5%	Fs
		T=-40 °C to +85 °C	-1%	--	1%	Fs
Power Consumption			--	12	--	uA
Vref Out Characteristics						
$Vref_{Accuracy}$	Vref Gain Accuracy	G=1	-0.2%	--	0.2%	
		G=2	-0.2%	--	0.2%	
		G=4	-0.2%	--	0.2%	
		G=5	-0.2%	--	0.2%	
$Vref_{offset}$	Vref Opamp Offset	G=1 (VCM IN=VDD/2)	-3.5	--	3.5	mV
Vref DAC_{offset}			--	7.5	--	mV
$I_{loading}$		Push Pull Output	2	--	--	mA
Power Consumption			--	10	--	uA
Voltage of Output to VDD		Maximum output voltage $\mathrm{Vout} = \mathrm{VDD} - 0.3 - 300\Omega \times \mathrm{Iout}$				
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

Table 8：I²C Pin Timing Parameter, (VDD: 1.8V±5%, Temp: -40℃ ~ 85℃)

Parameter	Description	Condition	Standard-Mode		Unit
			Min	Max	
F_{SCL}	Clock Frequency, SCL		--	100	KHz
t_{LOW}	Clock Pulse Width Low		4.7	--	us
t_{HIGH}	Clock Pulse Width High		4.0	--	us
t_I	Input Filter Spike Suppression (SCL,SDA)		--	70	ns
t_{AA}	Clock Low to Data Out Valid		--	3.45	us
t_{BUF}	Bus Free Time between Stop and Start		4.7	--	us
t_{HD_STA}	Start Hold Time		4.7	--	us
t_{SU_STA}	Start Set-up Time		4.7	--	us
t_{HD_DAT}	Data Hold Time		0	--	ns
t_{SU_DAT}	Data Set-up Time		250	--	ns
t_R	Inputs Fail Time		--	1000	ns
t_F	Inputs Rise Time		--	300	ns
t_{SU_STO}	Stop Set-up Time		4.0	--	us
t_{DH}	Data out Hold Time		50	--	ns
Note: Timing Diagram can be found in the Figure 18.					

Table 9：I²C Pin Timing Parameter, (VDD:2.3V ~ 5.5V, Temp: -40℃ ~ 85℃)

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	--	1000	KHz
t_{LOW}	Clock Pulse Width Low		1300	--	500	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	260	--	ns
t_I	Input Filter Spike Suppression (SCL,SDA)	VDD=2.5V±8%	--	95	--	168	ns
		VDD=3.3V±10%	--	95	--	157	ns
		VDD=5V±10%	--	111	--	156	ns
t_{AA}	Clock Low to Data Out Valid		--	900	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	500	--	ns
t_{HD_STA}	Start Hold Time		600	--	260	--	ns
t_{SU_STA}	Start Set-up Time		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time		0	--	0	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
t_R	Inputs Fail Time		--	300	--	120	ns
t_F	Inputs Rise Time		--	300	--	120	ns
t_{SU_STO}	Stop Set-up Time		600	--	260	--	ns
t_{DH}	Data out Hold Time		50	--	50	--	ns
Note: Timing Diagram can be found in the Figure 18.							

4. IO Pins

The LS98006 has a total of 17 GPIO Pins which can function as either a user-defined Input or Output, as well as serve as a special function (such as outputting the voltage reference) and 1 GPI Pin.

4.1 GPI Pin

GPI_0 serve as General Purpose Input Pin, it's internal block diagram is shown in Figure 3.

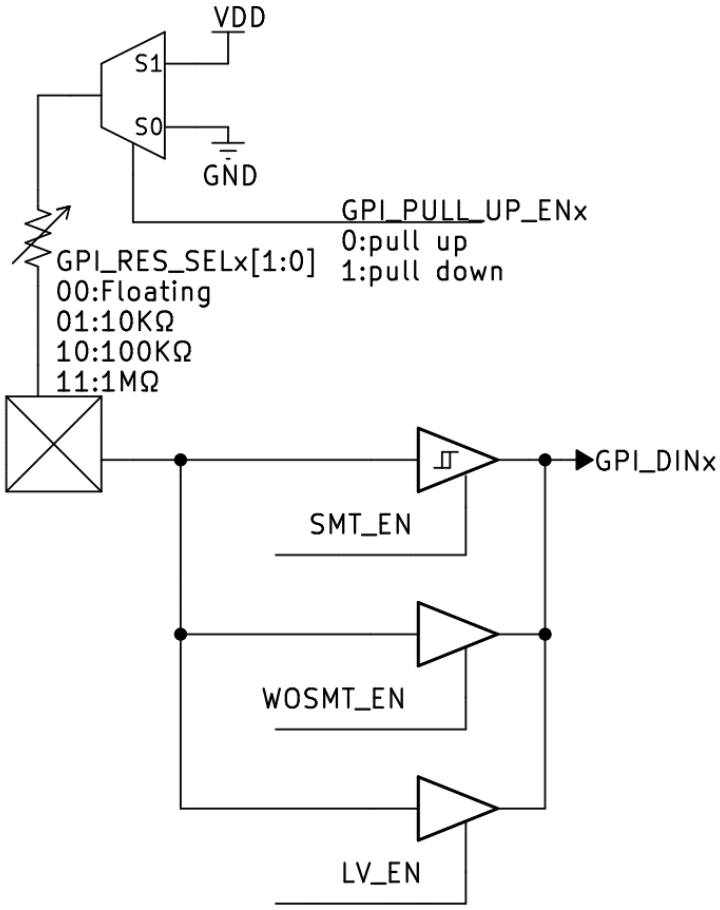


Figure 3: GPI0 Structure Diagram

4.2 GPIO Pins

GPIO_1、GPIO_2、GPIO_3、GPIO_4、GPIO_5、GPIO_6、GPIO_7、GPIO_8、GPIO_9、GPIO_10、GPIO_11、GP1O_12、GP1O_13、GPIO_14、GPIO_15、GPIO_16 and GPIO_17 serve as General Purpose IO Pins.

For the GPIO_6 and GPIO_7, which are applied to I²C-SCL and I²C-SDA, the system block diagram is shown in Figure 4.

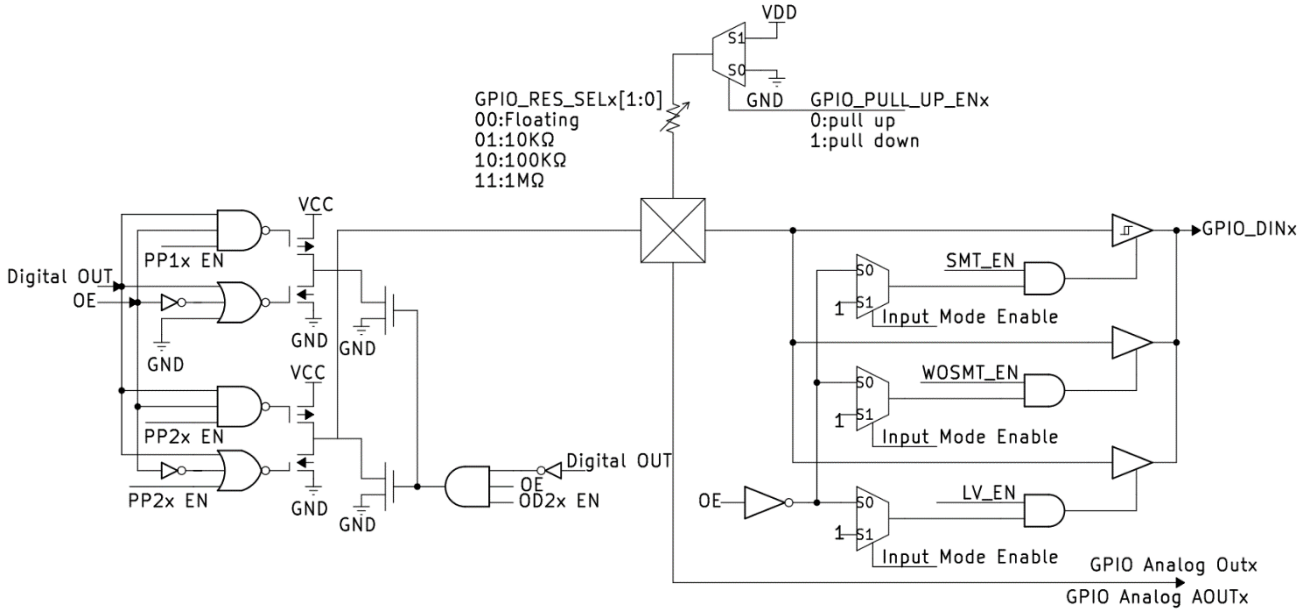


Figure 4：IO with I²C Mode IO Structure Diagram

For the GPIO_1,2,3,4,5,8,9,10,11,12,13,14,15,16 and 17, the system block diagram is shown in Figure 5.

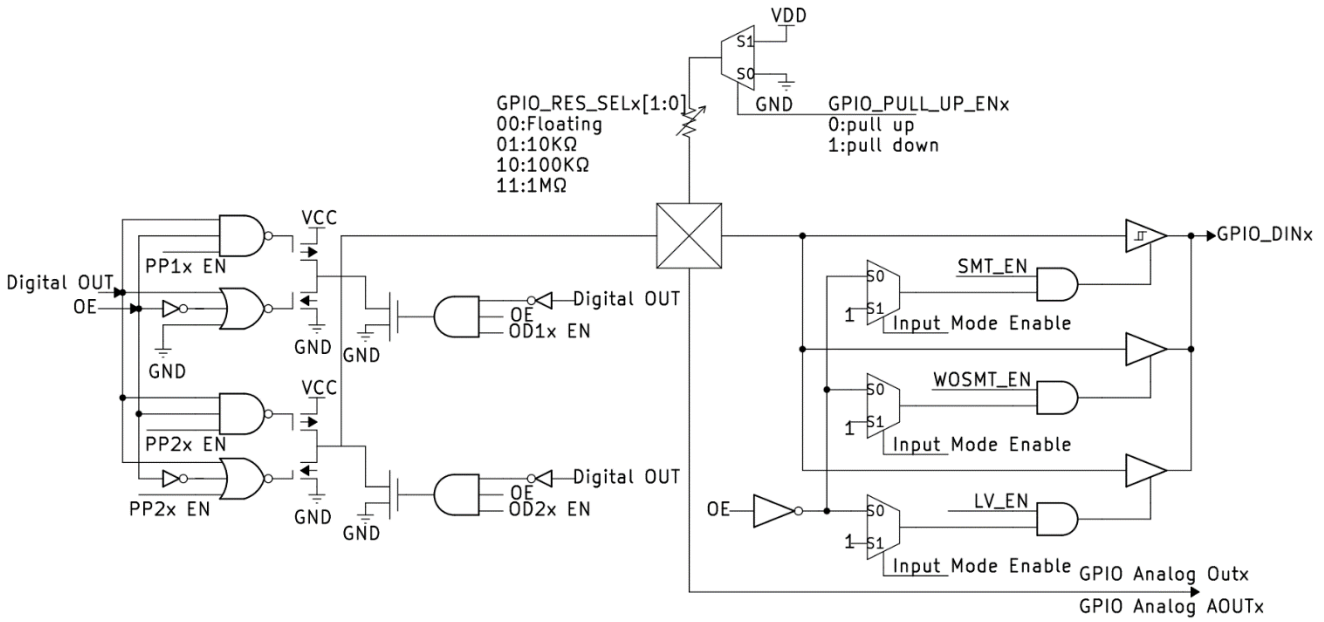


Figure 5：GPIO with OE Structure Diagram

5. Connection Matrix

LS98006 has an interconnection matrix internally, which can be used for internal resource connections and matrix connections through register configuration. These registers can be burned through OTP.

The input of the connection matrix comes from internal resources or the output of the connection matrix, while the output of the connection matrix is the input of internal resources or the connection matrix. The output of each connection matrix is configured through a set of registers.

6. Combination Function Macrocells

The LS98006 has thirty-nine combination function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells:

- Seven 2-bit LUT/DFF
- Three 2-bit LUT/Pattern Generator
- Six 2-bit LUT/Edge Detector
- Twenty 3-bit LUT/DFF with nSET/nRST
- Three 3-bit LUT/36-bit Pipe Delay

6.1 2-bit LUT/Pattern Generator

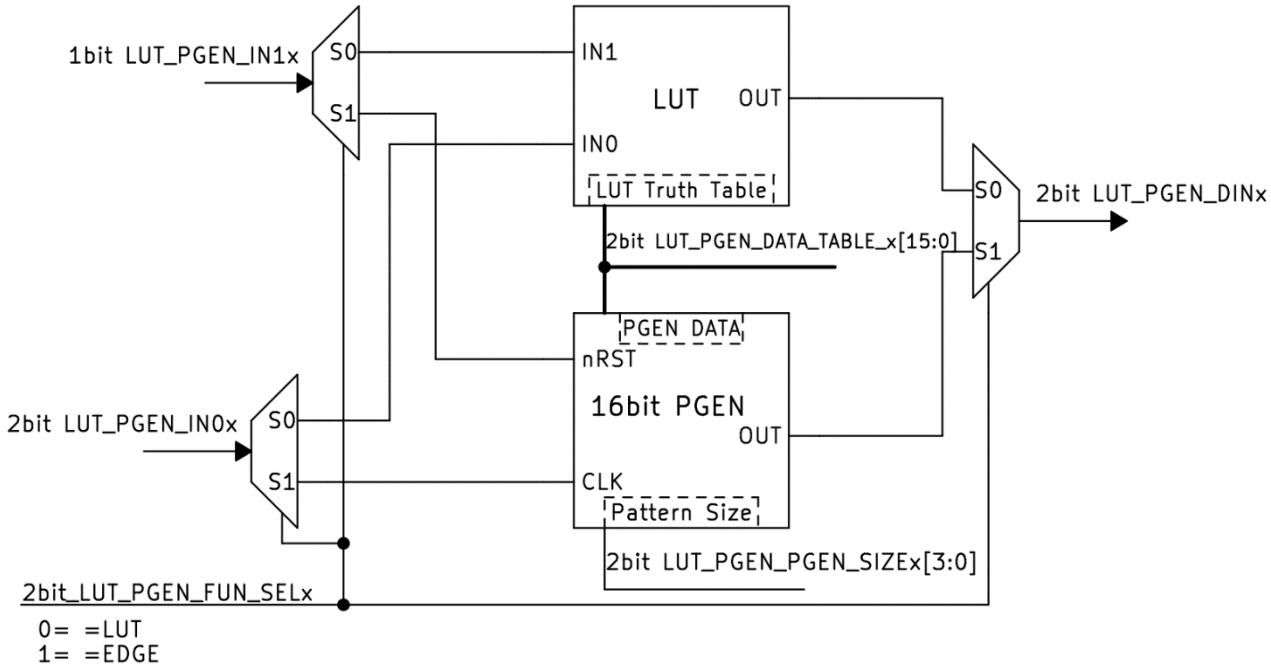


Figure 6：2-bit LUT/Pattern Generator

6.2 2-bit LUT/Edge Detector

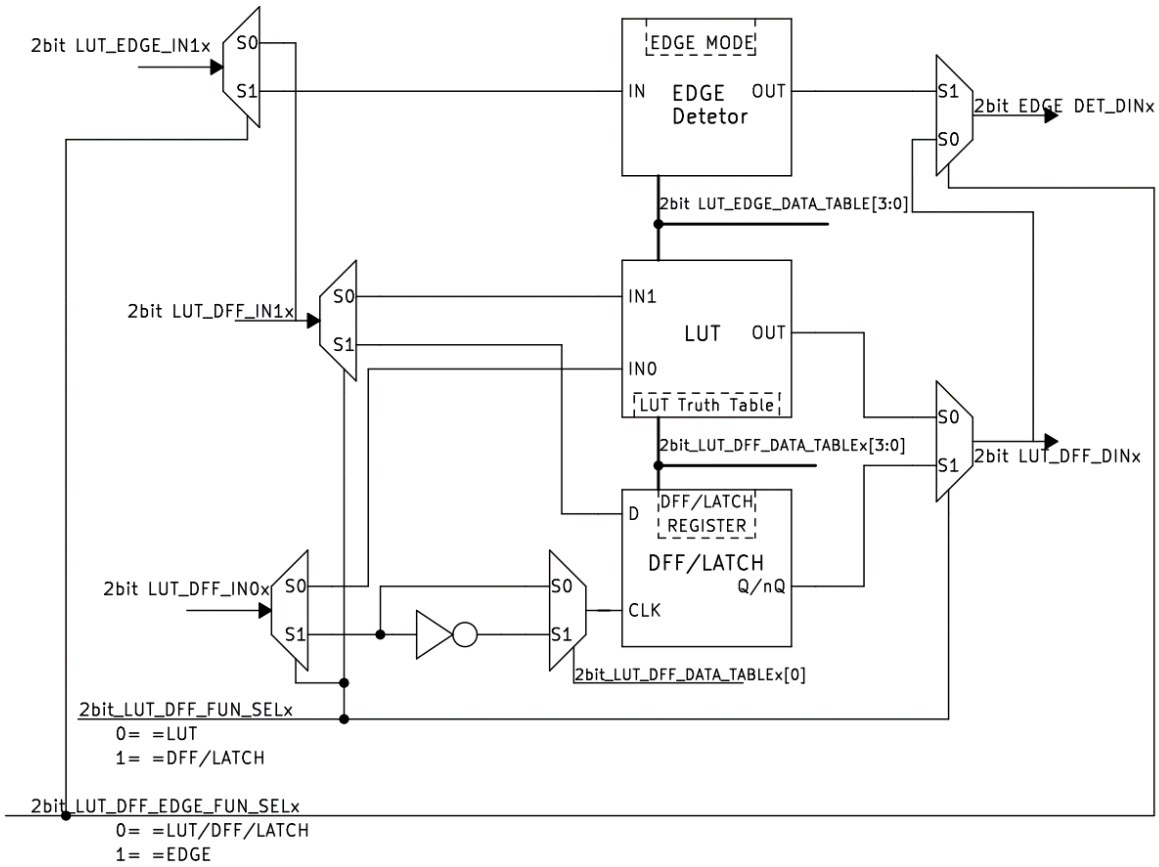


Figure 7：2-bit LUT/DFF/Edge Detector

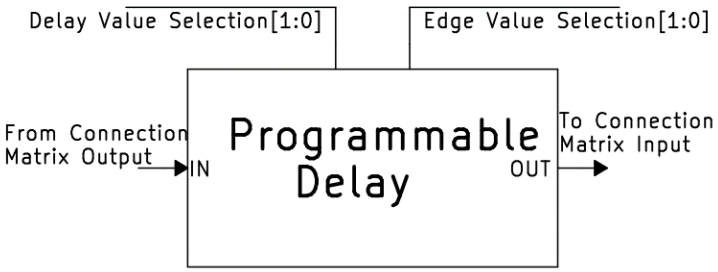


Figure 8：Programmable Delay

6.3 3-bit LUT/DFF with nSET/nRST or Pipe Delay

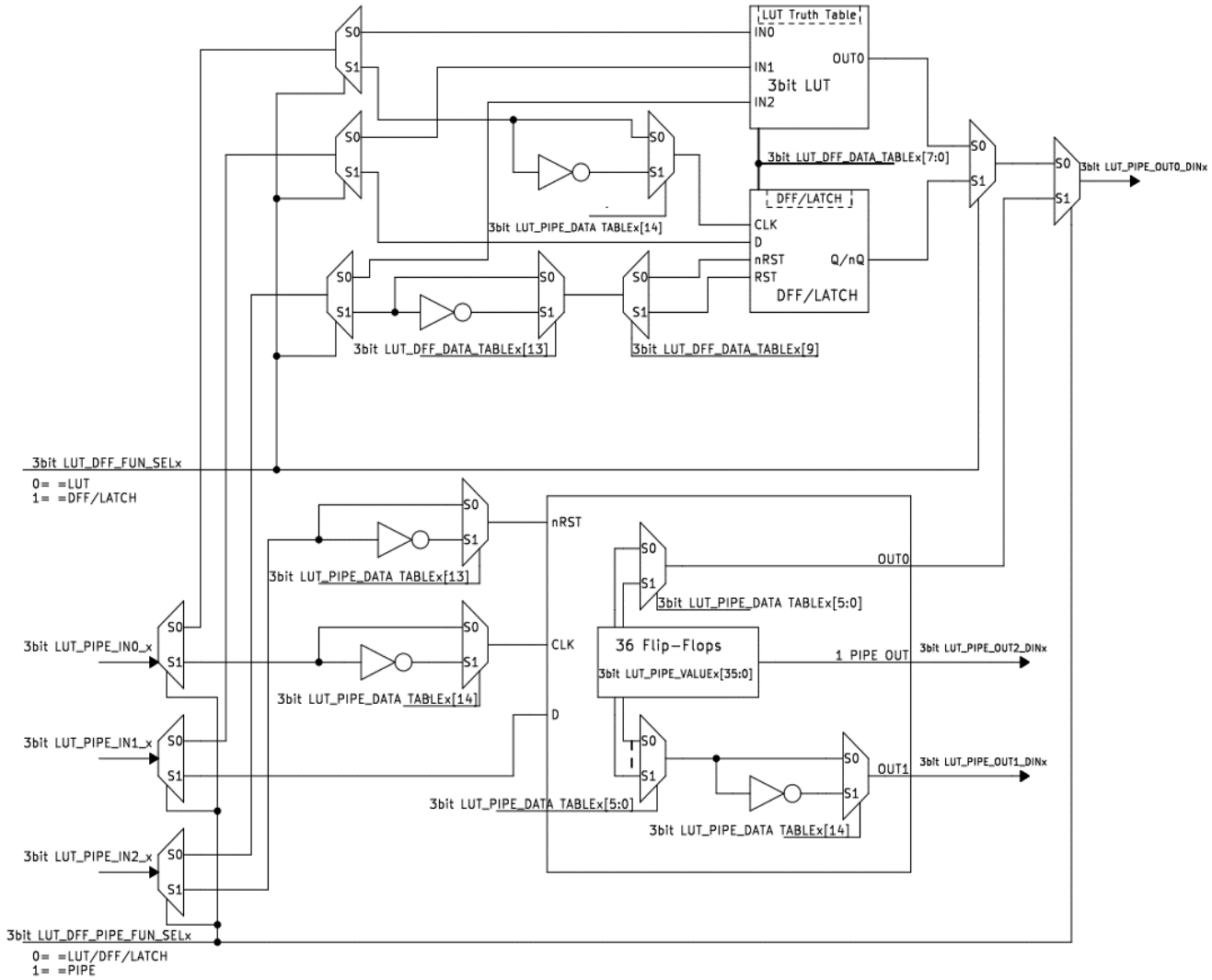


Figure 9：3-bit LUT/ DFF or Pipe Delay

7. Multi-Function Block（MFB）

LS98006 has sixteen Multi-Function Blocks that can serve as more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes s such as One Shot, Frequency Detect, Edge Detect, and others. Also, the block is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF.

See the list below for the functions that can be implemented in these blocks:

- Twelve Selectable 3-bit LUT/DFF + 8-bit Counter/Delay
- Four Selectable 4-bit LUT/DFF + 16-bit Counter/Delay

7.1 3-bit LUT/DFF or 8-bit Counter/Delay Block Diagrams

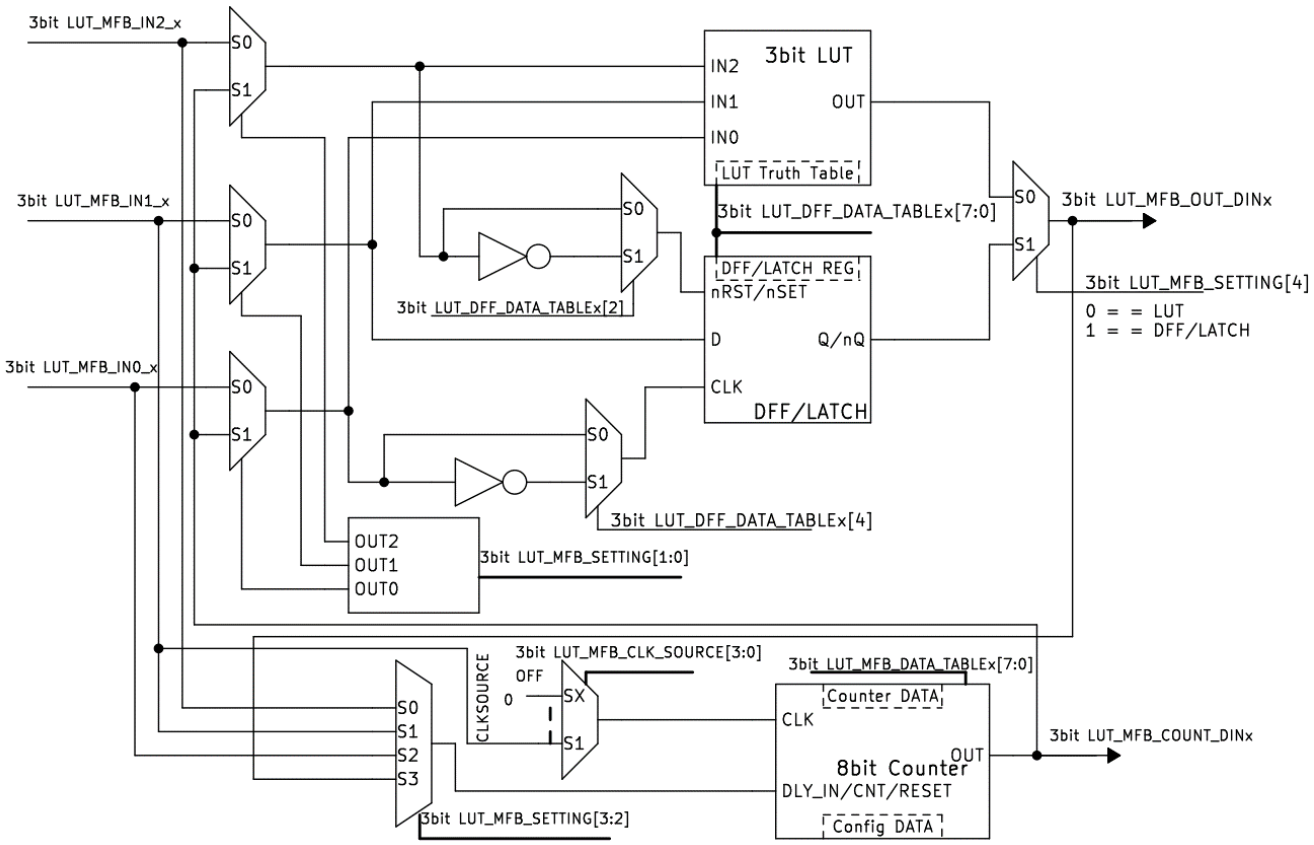


Figure 10：3-bit LUT/DFF or 8-bit Counter/Delay

7.2 4-bit LUT/DFF or 16-bit Counter/Delay Block Diagrams

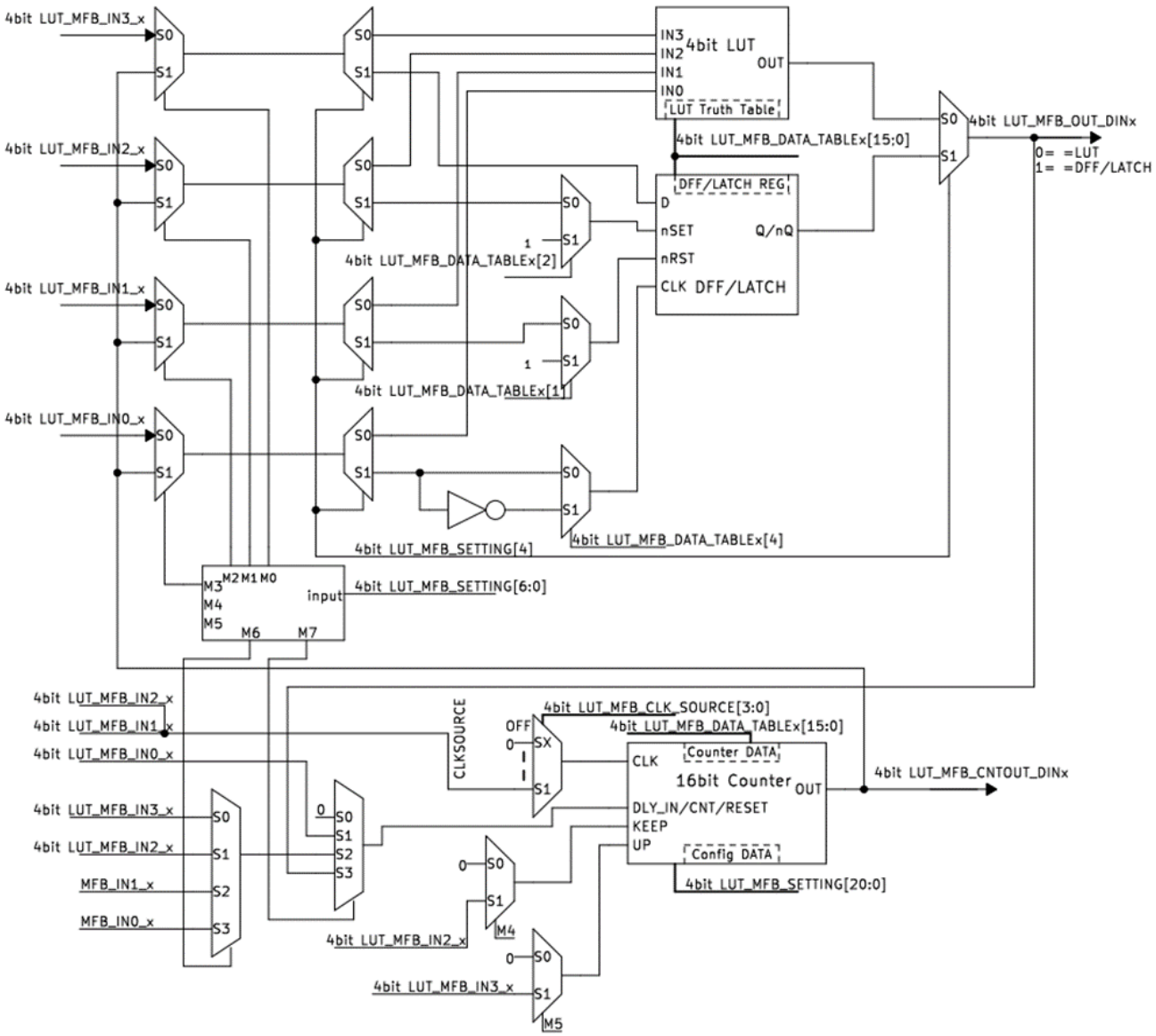


Figure 11：4-bit LUT/DFF or 16-bit Counter/Delay

8. I²C Virtual Memory Out and Pipe Delay

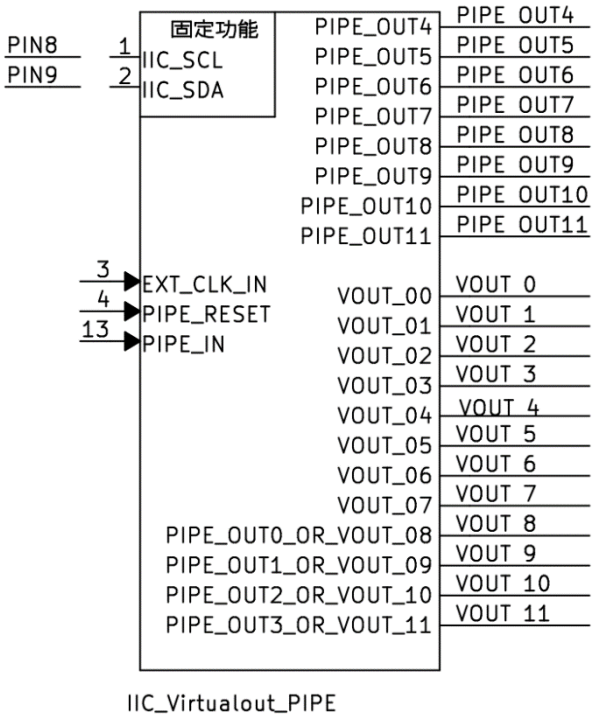


Figure 12：(a) I²C Virtual Memory Out and Pipe Delay diagram

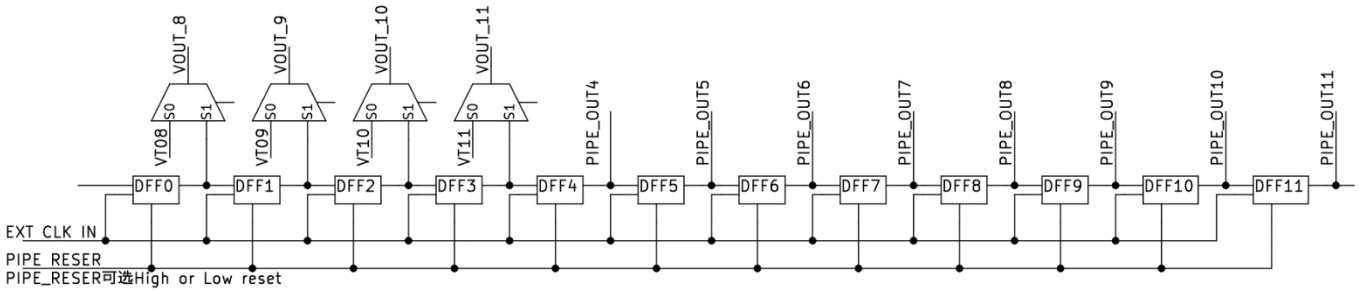


Figure 12：(b) I²C Virtual Memory Out and Pipe Delay

Legend:
Pipe-Reset can select High or Low Reset Mode
Pipe In can select any Data input in DFF0-4
The virtual output and Pipe Delay sharing an 8-bit output
VT08-VT11 are outputs of I²C Virtual Output which can select Virtual Output or Pipe Output

9. I²C Communication Interface

The LS98006 provides an I²C communication interface that allows the I²C master to read or write internal registers, thereby remotely reconfiguring internal resources and their connection relationships.

9.1 I²C Read

9.1.1 Current Address Read Command

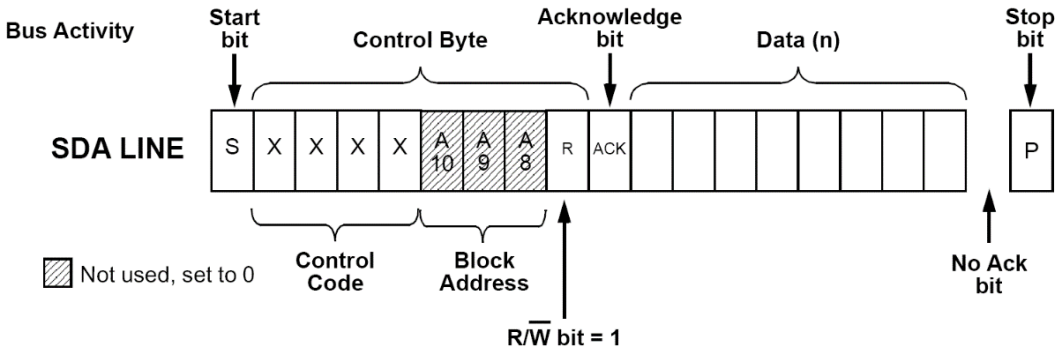


Figure 13：Current Address Read Command

9.1.2 Random Read Command

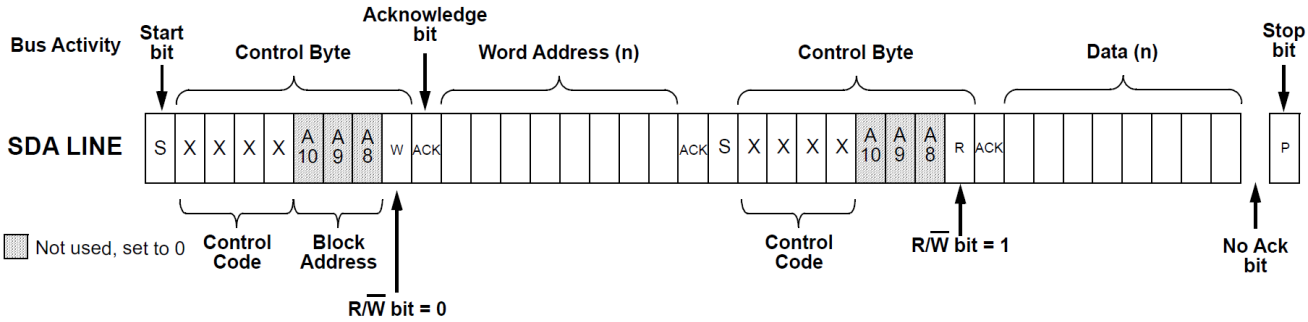


Figure 14：Random Read Command

9.1.3 Sequential Read Command

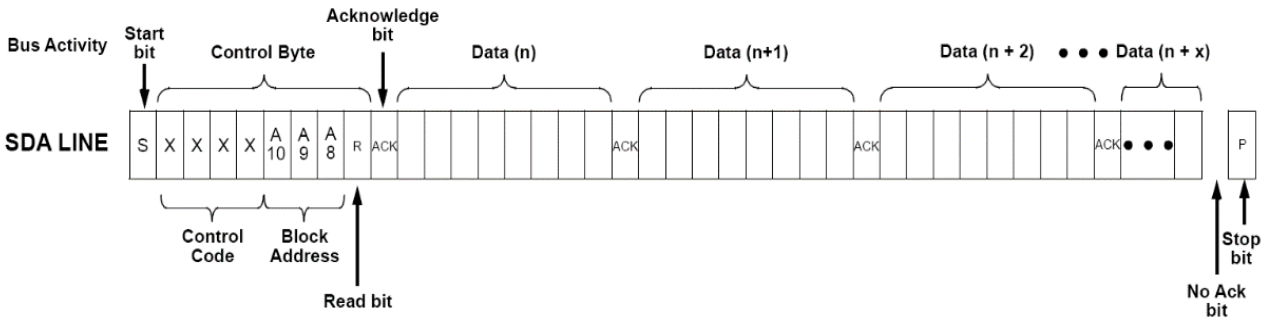


Figure 15：Sequential Read Command

9.2 I²C Write

9.2.1 Byte Write Command

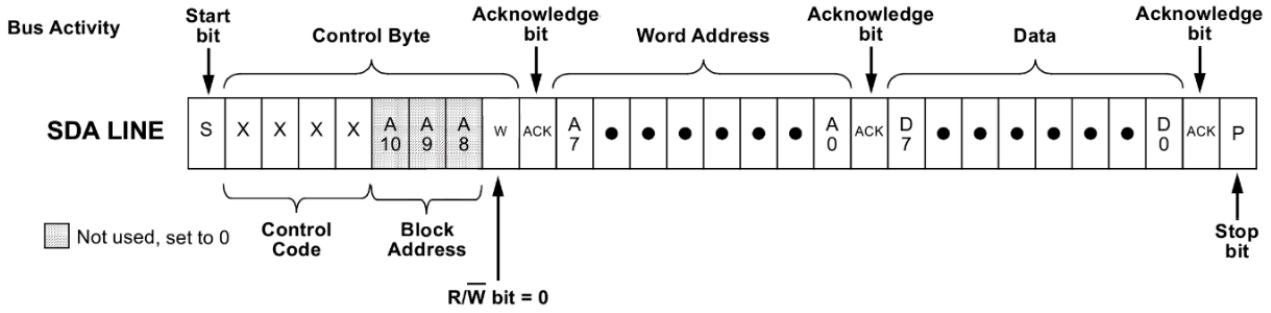


Figure 16：Byte Write Command

9.2.2 Sequential Write Command

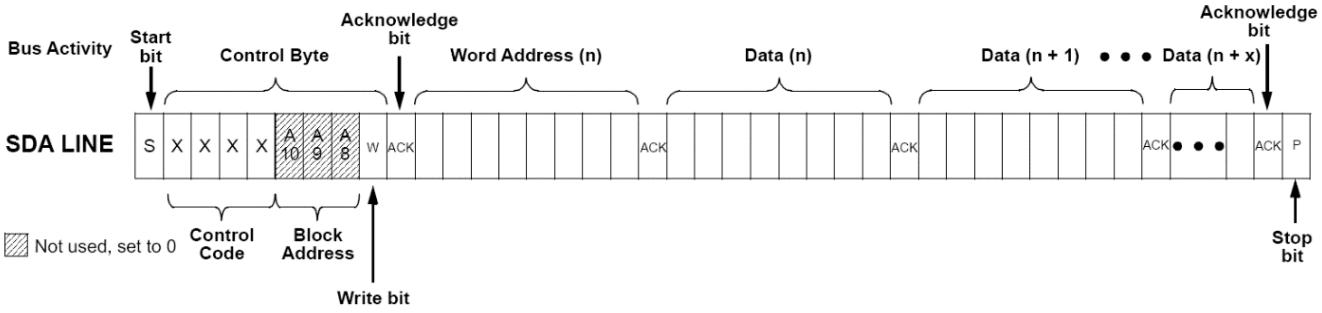


Figure 17：Sequential Write Command

9.3 I²C Timing Diagram

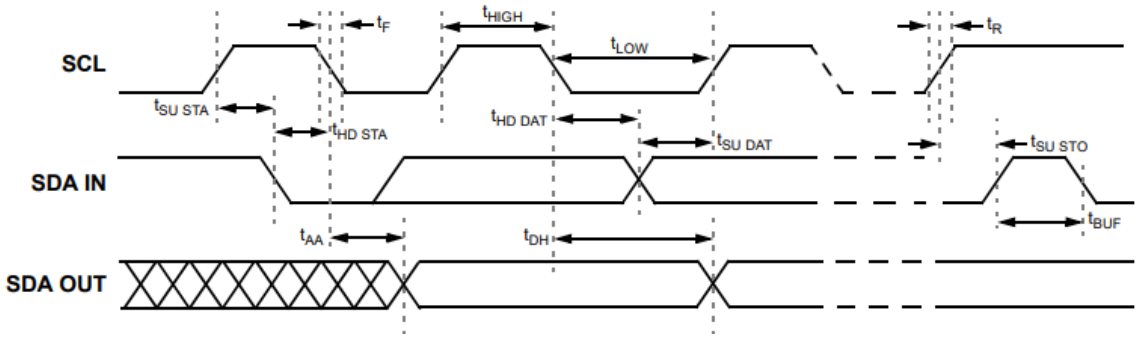


Figure 18：I²C Timing Diagram

9.4 I²C Software Reset Function

If the I²C serial communication is established, the device can be reset to its initial power-on conditions, including the configuration of all Macrocells and all connections provided by the connection matrix. It is achieved by setting register [2922] and resetting I²C to "1", which causes the device to enable again the POR sequence, including reloading all register data from NVM. During the POR sequence, the output of the device will be in tristate, and after the reset is completed, the value of the content register [2922] will be automatically set to "0".

10. Voltage Reference (Vref)

10.1 Voltage Reference Overview

The voltage source output macrocell, with Voltage Reference from an 8 Bit DAC, is connected to a drive amplifier with an rail to rail output capacity of 1X, 2X, 4X, 5X.

10.2 Voltage Reference Source Formula

Vref =1V/256*（D+1）*Gain （D:8 Bit DAC’s Data Gain: ×1 ×2 ×4 ×5）

10.3 Voltage Reference Block Diagram

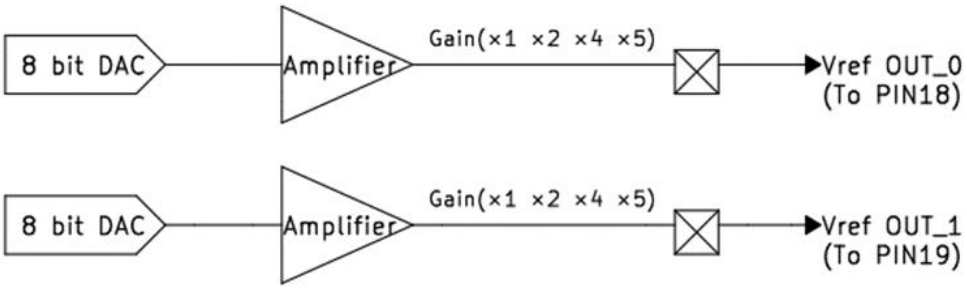


Figure 19：Voltage Reference Block Diagram

11. Constant Current Source (Current Source maximum 3mA）

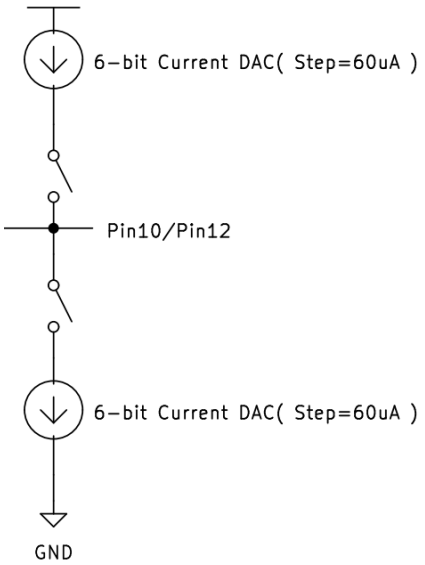


Figure 20：Constant Current Source diagram

12. Analog Comparator (ACMP)

12.1 Multi-channel Sampling Analog Comparator(MACMP)

The input of MACMP has 8 channels. After the multi-channel function is enabled, the multi-channel can be 2 or 3 or 4 channels, and each channel can select any of the 8 input channels.

- Internal VREF: 8bit DAC (=1V*‘DAC data+1’/256)

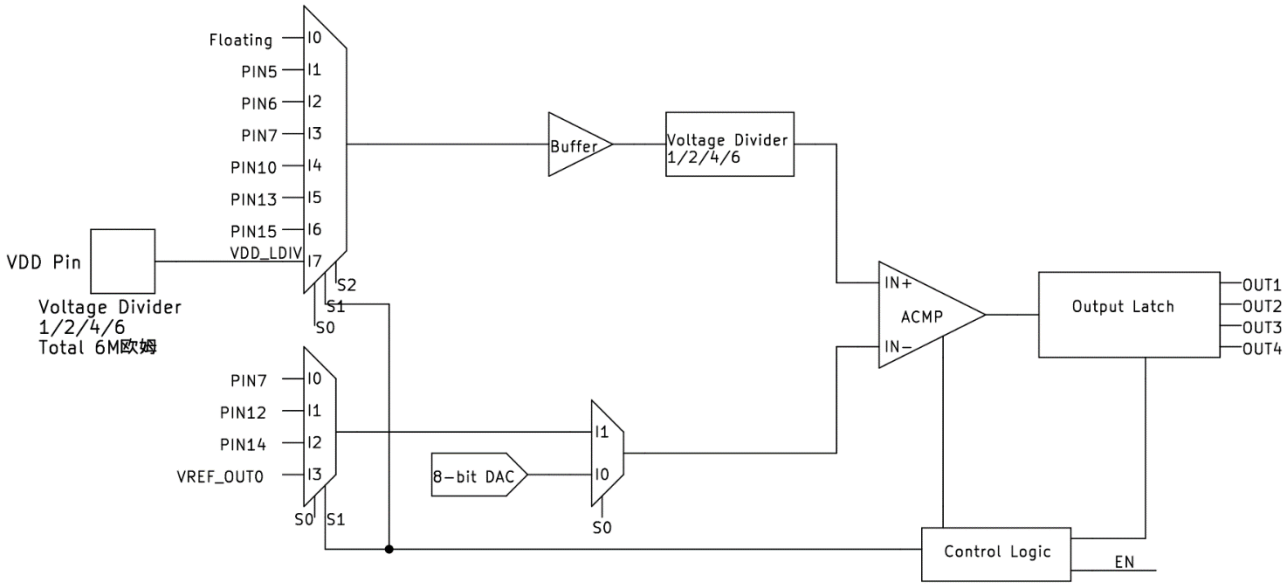


Figure 21：Multi-channel Analog Comparator

12.2 Single-channel Analog Comparator 1(ACMP1)

- Internal VREF: 8bit DAC (=1V*‘DAC data+1’/256)

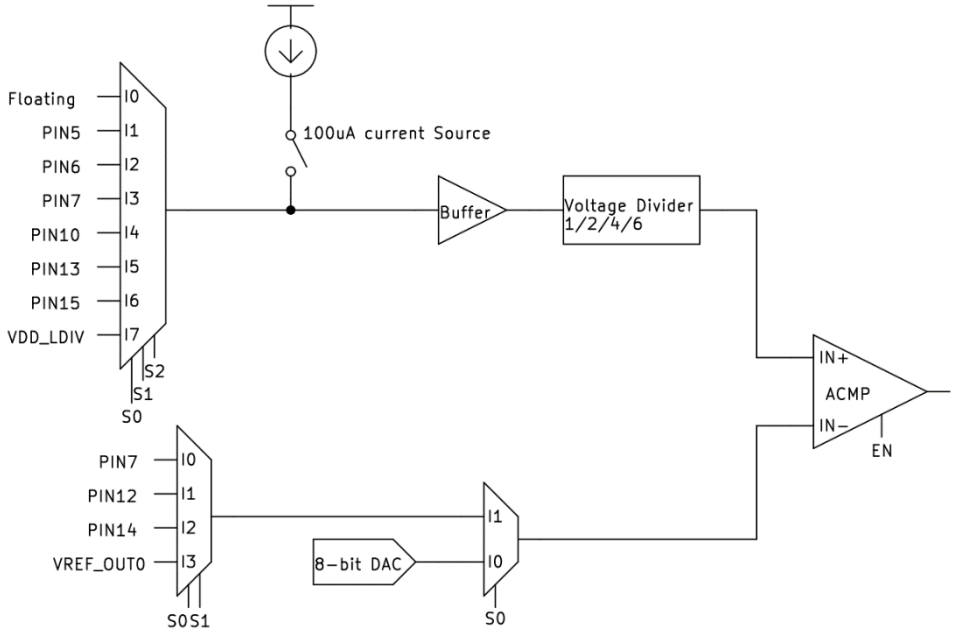


Figure 22：Single-channel Analog Comparator 1

12.3 Single-channel Analog Comparator 2(ACMP2)

- Internal VREF: 8bit DAC (=1V*‘DAC data+1’/256)

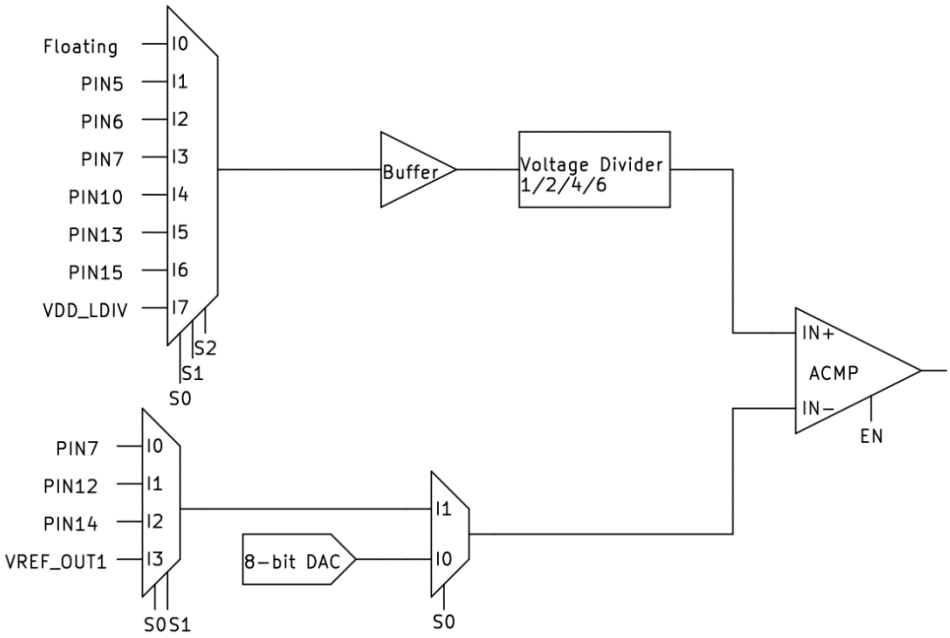


Figure 23：Single-channel Analog Comparator 2

13. Clock Schem

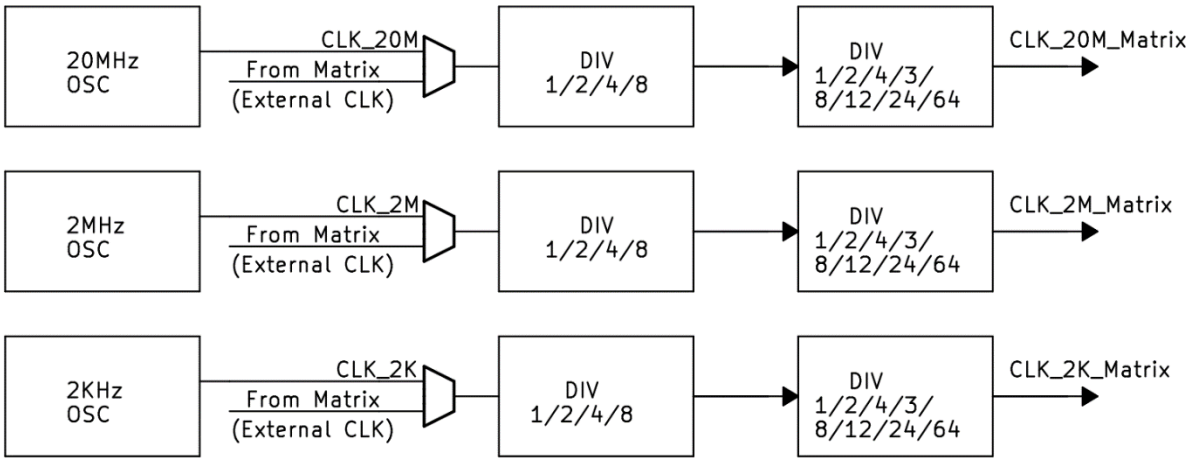


Figure 24：Clock Schem

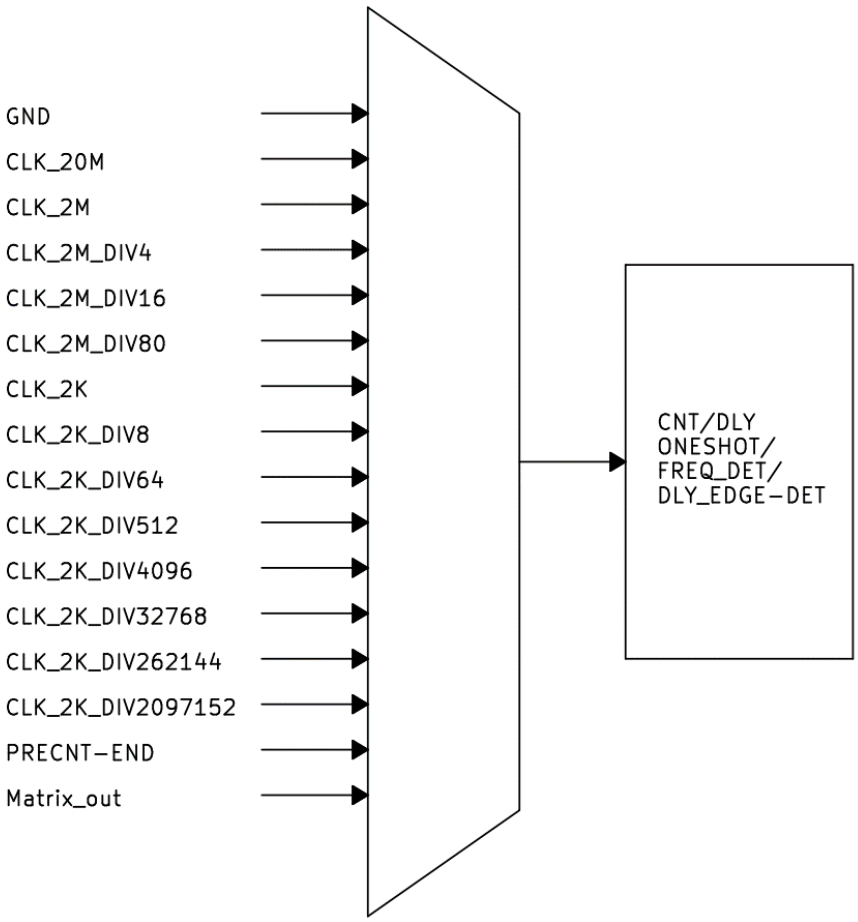


Figure 25：Clock allocation diagram

14. External Clock

LS98006 supports multiple ways to use external high-precision clocks as internal operation reference sources.

14.1 Matrix Source for 2KHz / 2MHz / 20MHz Clock

When the external clock function is enabled, the clock comes from the interconnection matrix.

15. Crystal Oscillator

The crystal oscillator has three operating modes, as shown in Figure 26, selected through register.

The first working mode: XTAL0 for high-speed mode
The second working mode: XTAL1 for low-power (1uA) RTC
Third operating mode: XTAL2 for low-power (1.5uA) RTC

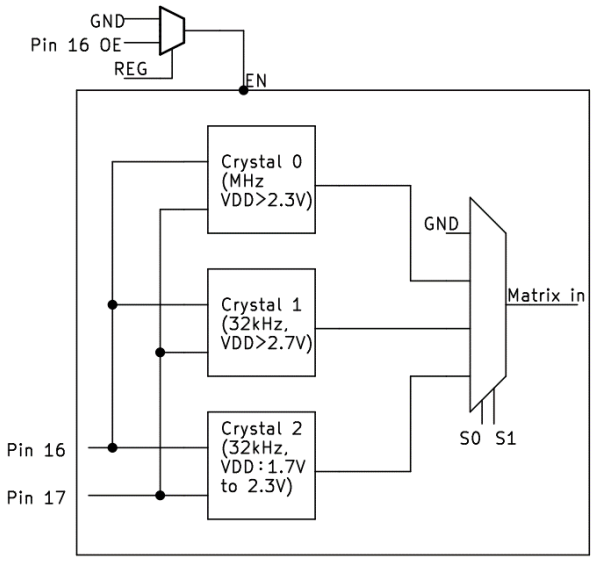


Figure 26：Crystal Oscillator block diagram

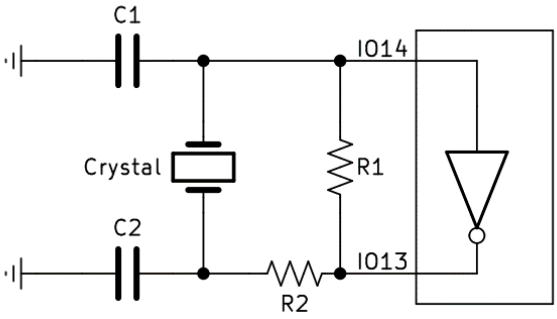


Figure 27：Crystal Oscillator

Table 10 ：External Components Selection Table

f	C1	C2	R1	R2
32.768kHz	5pF	5pF	10MΩ	100Ω
4-40MHz	10pF	10pF	1MΩ	100Ω

Note: At 32.768kHz, the resistance R1 is 8 MΩ~20 MΩ; Simultaneously ensuring that the RC product is a constant value (10 MΩ* 5pF).

16. Code Protection Function

LS98006 provides the customer with a code protection function, when the protection bit [2924] is program into "1", then all chip function related code can be locked, can not be read out, effectively protect the customer's design information.

17. POR Sequence

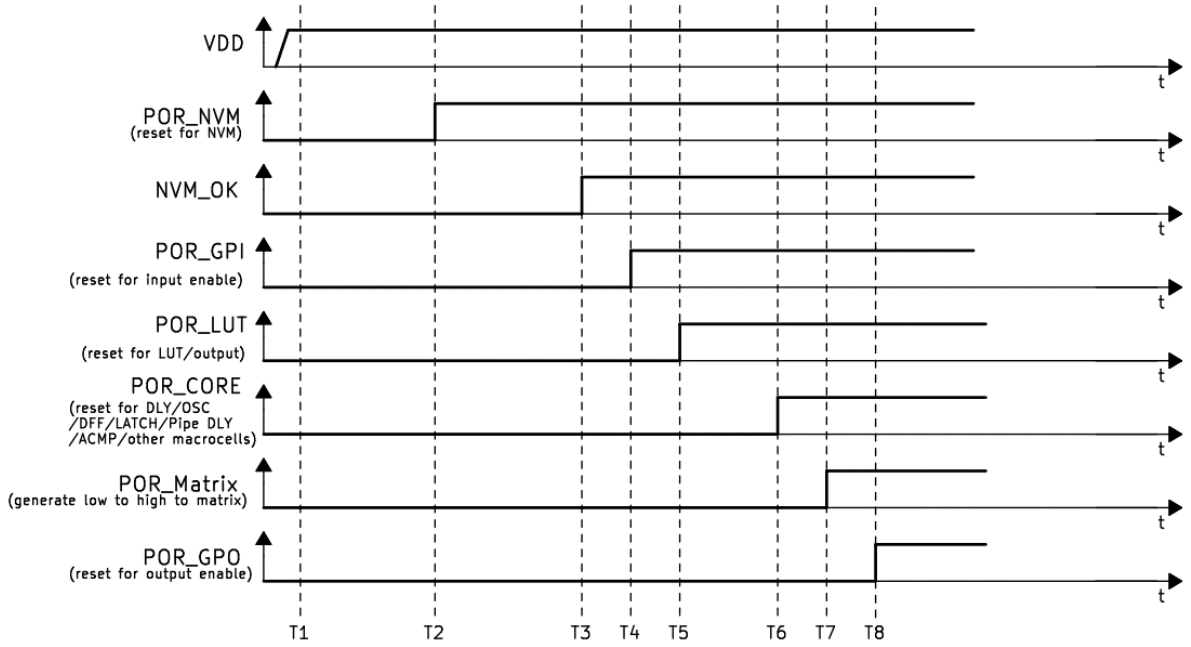


Figure 28：POR Sequence

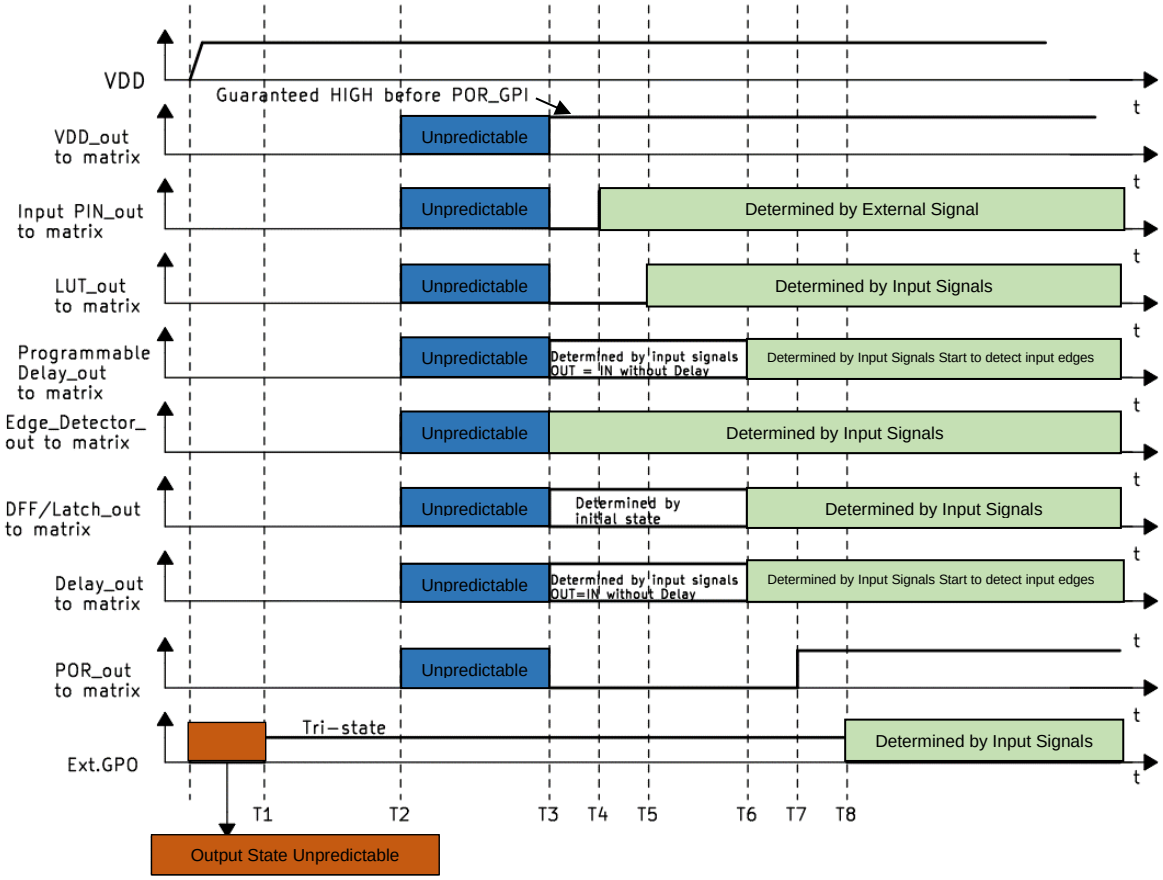


Figure 29：Internal Macrocell States during POR sequence

Note: T1-T8 in Figure 28 and Figure 29 correspond one-to-one.

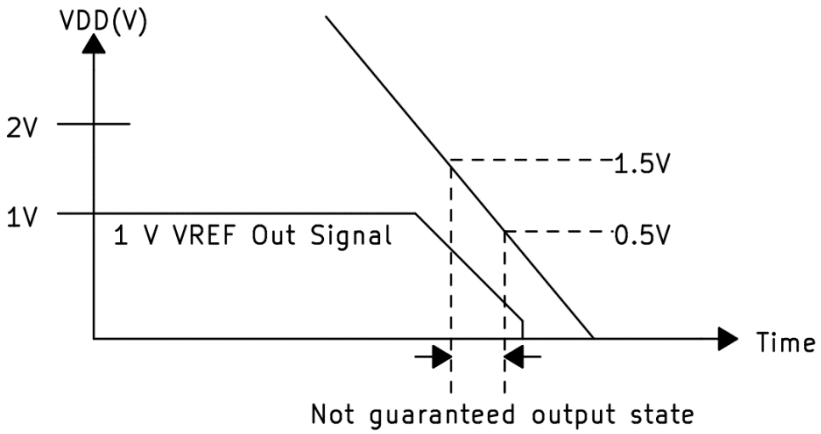


Figure 30：Power Down

During the power down process, when the VDD drops below the Power off Threshold, all macrocells in the LS98006 will be close down. Please take notice that during the slow frequency down period, the output may switch states during this period.

18. Virtual Memory

18.1 Virtual Memory Input

I²C can write register bit [2851:2840] into the input of the main matrix <75:64>.

18.2 Virtual Memory Output

I²C can read the output of internal nodes through register [2887:2872], and the following is the relevant configuration information：

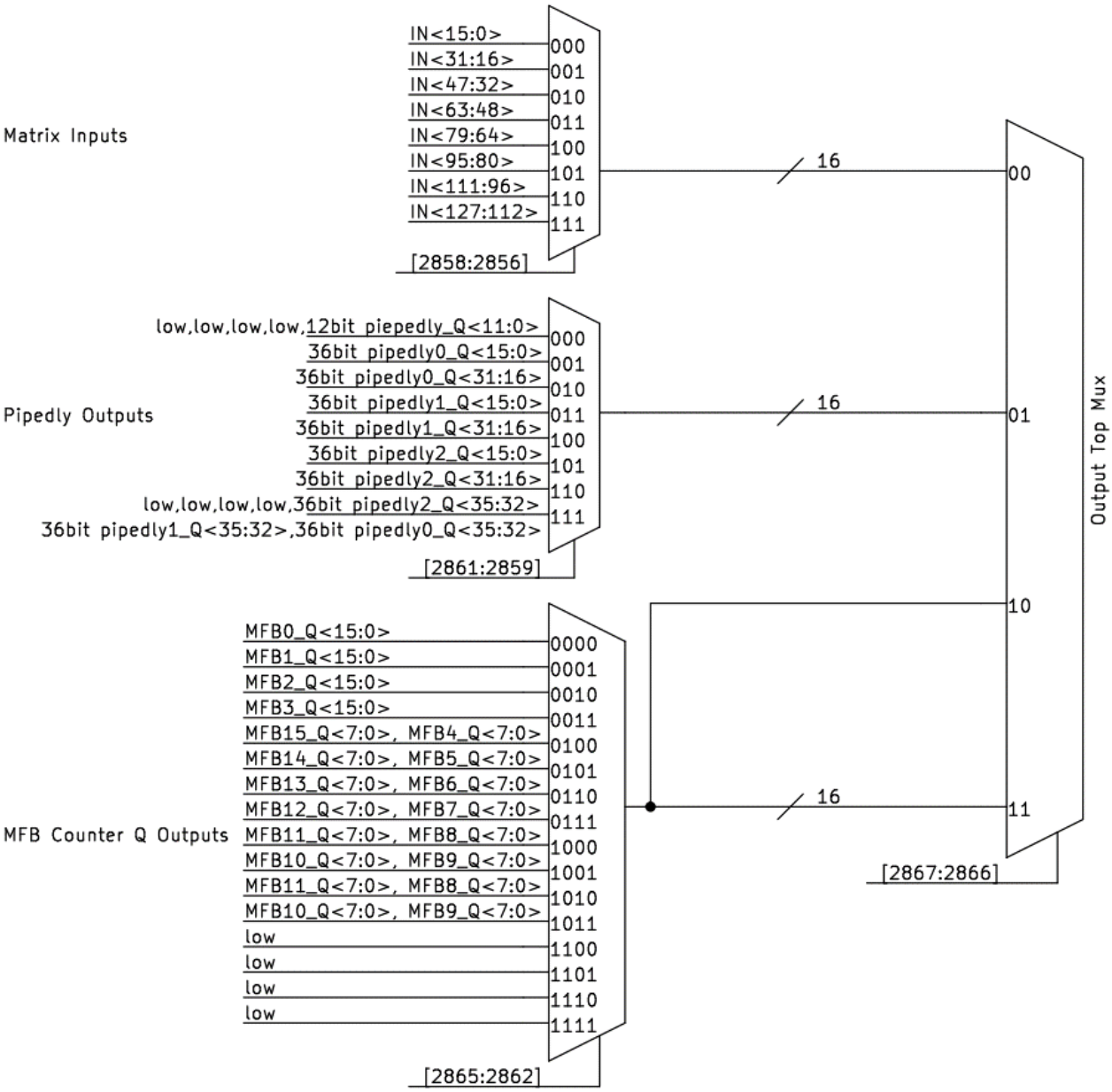
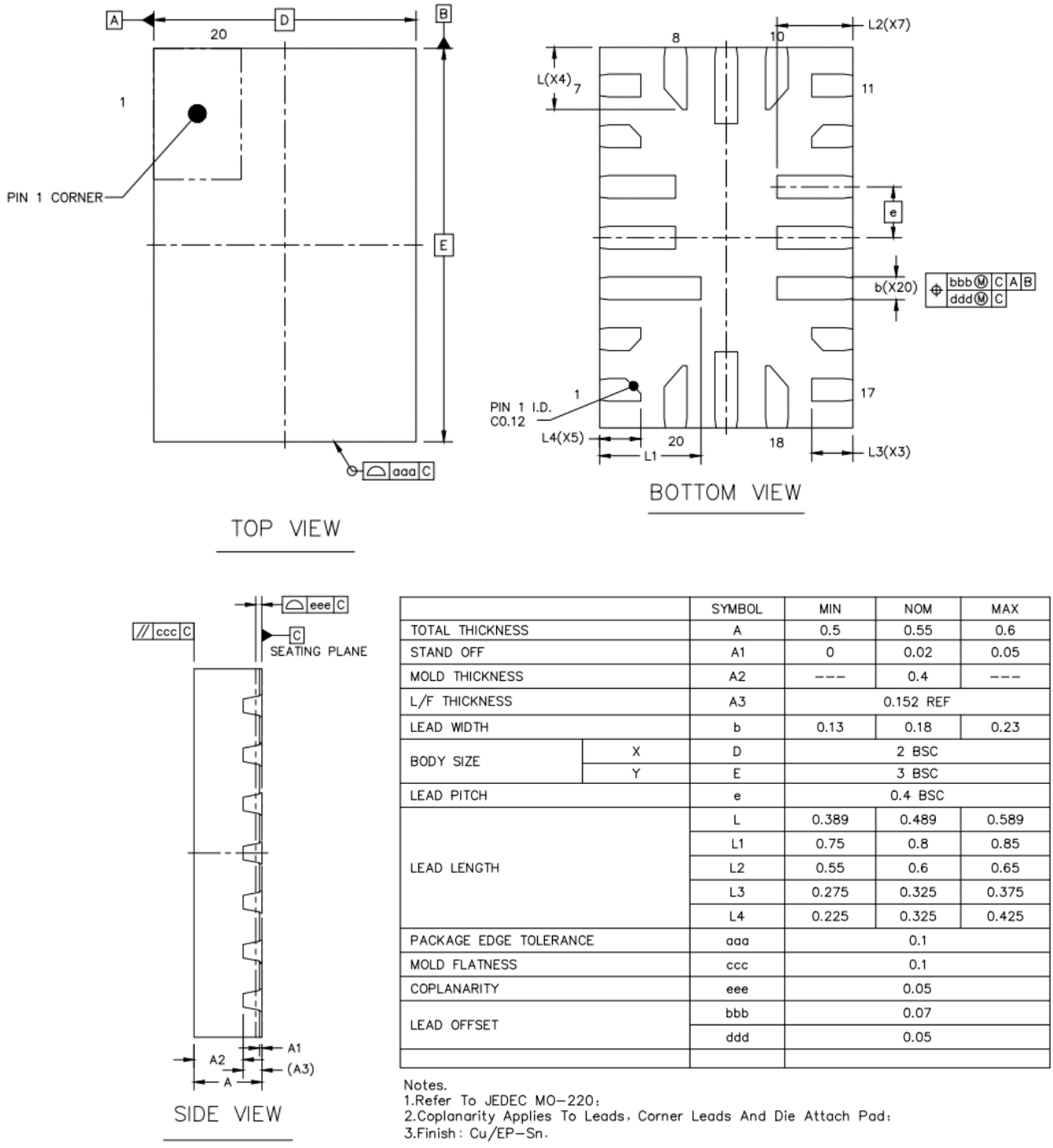


Figure 31：Virtual Memory Out

19. Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		2 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.4 BSC	
LEAD LENGTH		L	0.389	0.489	0.589
		L1	0.75	0.8	0.85
		L2	0.55	0.6	0.65
		L3	0.275	0.325	0.375
		L4	0.225	0.325	0.425
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	

Notes.
1.Refer To JEDEC MO-220;
2.Coplanarity Applies To Leads, Corner Leads And Die Attach Pad;
3.Finish: Cu/EP-Sn.

Figure 32：Package Outline Diagram

20. Ordering Information

20.1 Tape and Reel Specifications

Table 11：Package Type

Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
TQFN-20L 2.0×3.0mm	20	2.0×3.0×0.55	3000	3000	178/54	30	120	140	560	8	4

20.2 Carrier Tape Drawing and Dimensions

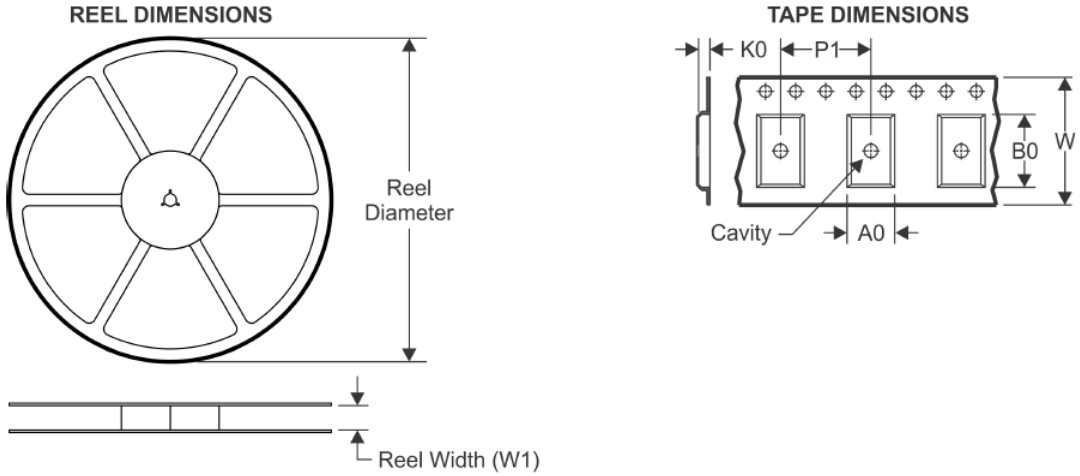


Figure 33：Carrier Tape Drawing and Dimensions

Table 12：Carrier Tape Drawing and Dimensions

A0	Dimension designed to accommodate the component width	2.30mm
B0	Dimension designed to accommodate the component length	3.30mm
K0	Dimension designed to accommodate the component thickness	0.75mm
W	Overall width of the carrier tape	8.00mm
W1	Reel Width	9.50mm
P0	Pitch between Index Hole Pitch	4.00mm
P1	Pitch between successive cavity centers	4.00mm

21. Revision History

Table 13：Revision History

Version	Revision Contents	Revised By	Date
R01	Initial version		2023-10-19
R02	1.Output PIN identification of Vref_out0 and Vref_out1 in Figure 19 (P27).		2023-12-06
R03	1.Optimize the PIN name annotation in the Top View diagram in Figure 2 (P7) and update the name synchronously with the PIN description that appears later.		2024-01-06
R04	1.Update Figure 26, add Crystal 2 working mode, change Tables 14 'C1 and C2' from '1pF' to '5pF', add annotations (P31). 2. Update Figure 29 to be colored (P32)		2024-03-18